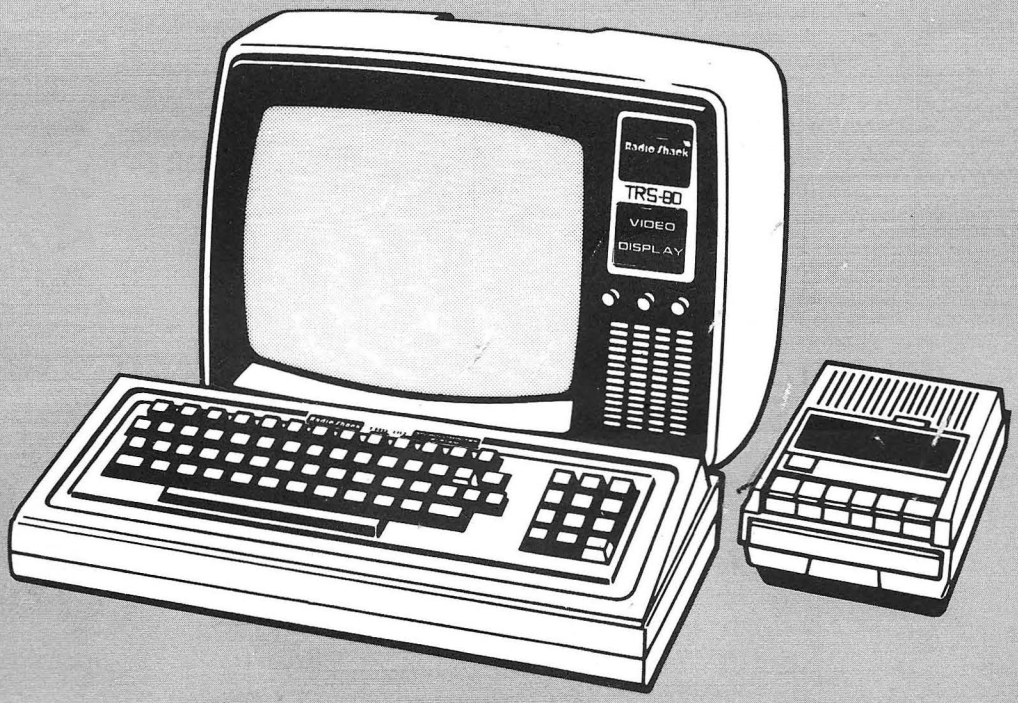
Radio Shack®

Service Manual

26-1003A/1006A/7016A

TRS-80
MICRO COMPUTER SYSTEM

Catalog Number: 26-1003A
1006A
7016A



CUSTOM MANUFACTURED FOR TANDY CORPORATION

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1. INTRODUCTION

In the systems employing microcomputers, TRS-80 was the earliest to appear on the market and has become one of the best sellers in many of the countries.

This is the result of the outstanding hardware composition and the abundant software service available. In particular, the BASIC LEVEL II and the readily prepared easy-to-use programs have won wide acclaim.

This Manual has been prepared for two purposes. One of them is to enable the purchaser of the TRS-80 Microcomputer himself to make adjustments or to deepen his understanding of the hardware. The other is for the use of our own servicemen in the repair of the microcomputer in the event trouble should develop.

However, if the microcomputer purchased by you fails to operate properly, do not attempt to repair it if you do not have sufficient confidence in mechanical matters. In case the microcomputer should become damaged by attempted repairs, there could be cases where we will not assume responsibility.

2. TRS-80 OUTLINE DESCRIPTION

The TRS-80 Microcomputer in its minimum composition consists of the main body, CRT display, and cassette recorder. By connecting optional Expansion Interfaces, it becomes possible to connect peripheral devices such as minifloppy, line printer, and RS232C serial interface board. However, in this manual, only the TRS-80 main unit and the minimum system will be covered.

For the TRS-80 cassette recorder, the special cassette recorder CTR-80 is used. The TRS-80 has been made to also allow use of general cassette recorder available on the market, but the use of exclusive cassette recorder CTR-80 will be found more convenient.

The TRS-80 employs μPD780 as its CPU (Central Processing Unit). The overall system composition is as shown in Fig. 2-1. (The μPD780 is identical with the Z80 made by Zilog Co., and can be replaced by Z80 with no problem.)

The CPU is the heart of the system that performs the calculations and the controls. There are 8 data buses and 16 address buses coming from the CPU; together with the control lines, they are connected to the principal parts. These are employed by the CPU to designate the places to store/retrieve the data and to transact the data.

The feature of the TRS-80 is that the keyboard, RAM, and others are memory-mapped. Address designations from 0000 to FFFF is possible with μPD780 (Z80), but inside the TRS-80 main body, address designations are made for 0000 to 7FFF only. The remaining 8000 to FFFF are address designated in the expansion interface RAM32K. The memory map is shown in Fig. 2-2.

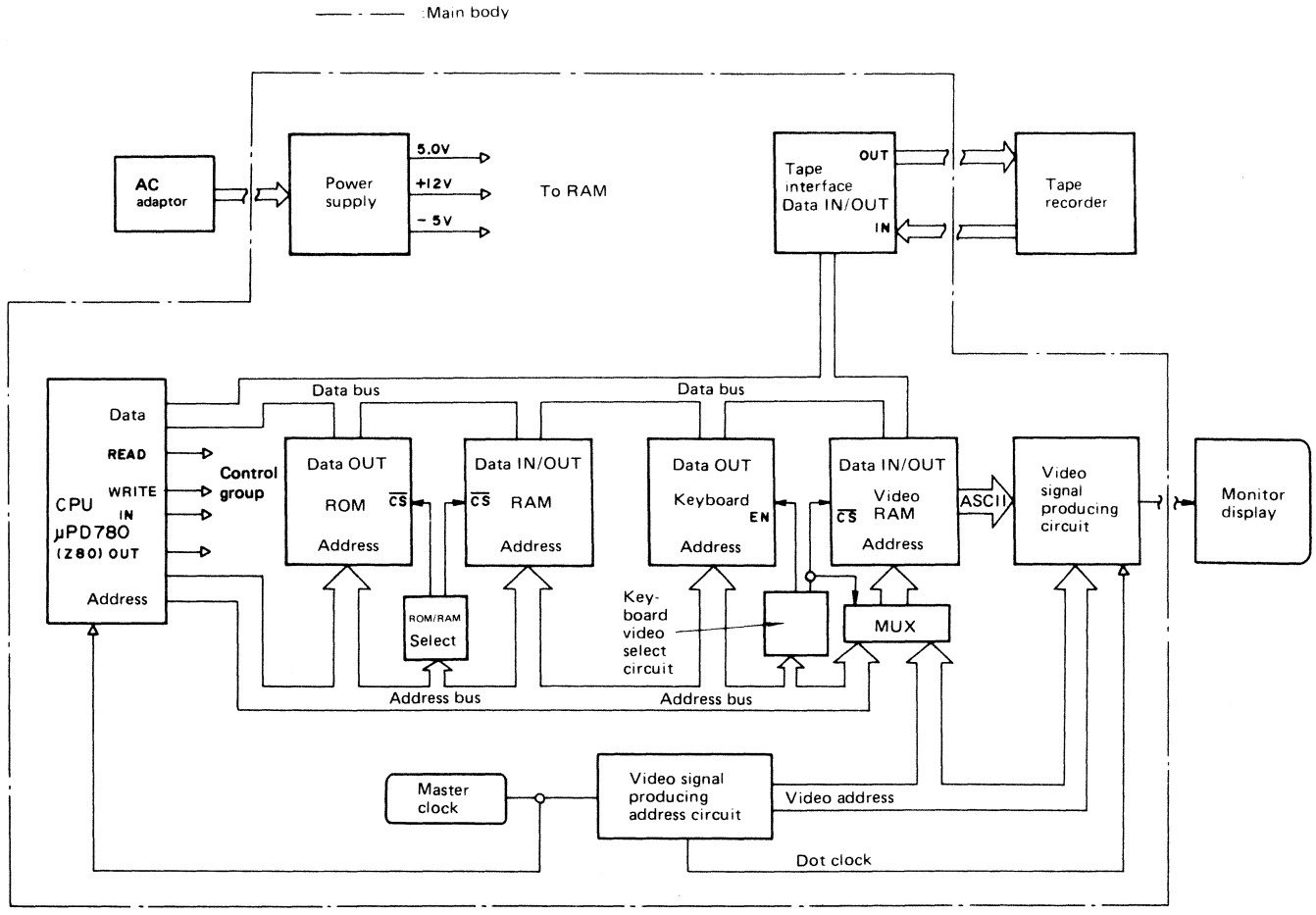


Figure 2-1. TRS-80 SYSTEM BLOCK DIAGRAM

The clock for operating the entire TRS-80 is a crystal oscillator that produces frequency of 10.6445 MHz. This is passed through the buffer and waveform shaped, and utilized in video signal generation circuit and CPU clock pulse. For the CPU clock pulse, this is divided by 6 by the counter to about 1.774 MHz.

The TRS-80 memories are ROM (Read Only Memory) consisting of 4K byte (in Basic Level I,) 12K byte (in Basic Level II,) or 13K byte (in Basic Level II Kana,) and RAM (Random Access Memory) consisting of 16K byte dynamic. Aside from these, there is a dynamic purpose RAM (1K byte) but this is not a part of the main memory.

The above is an outline description of the TRS-80. The operations of the various components will be covered in greater detail in Chap. 3.

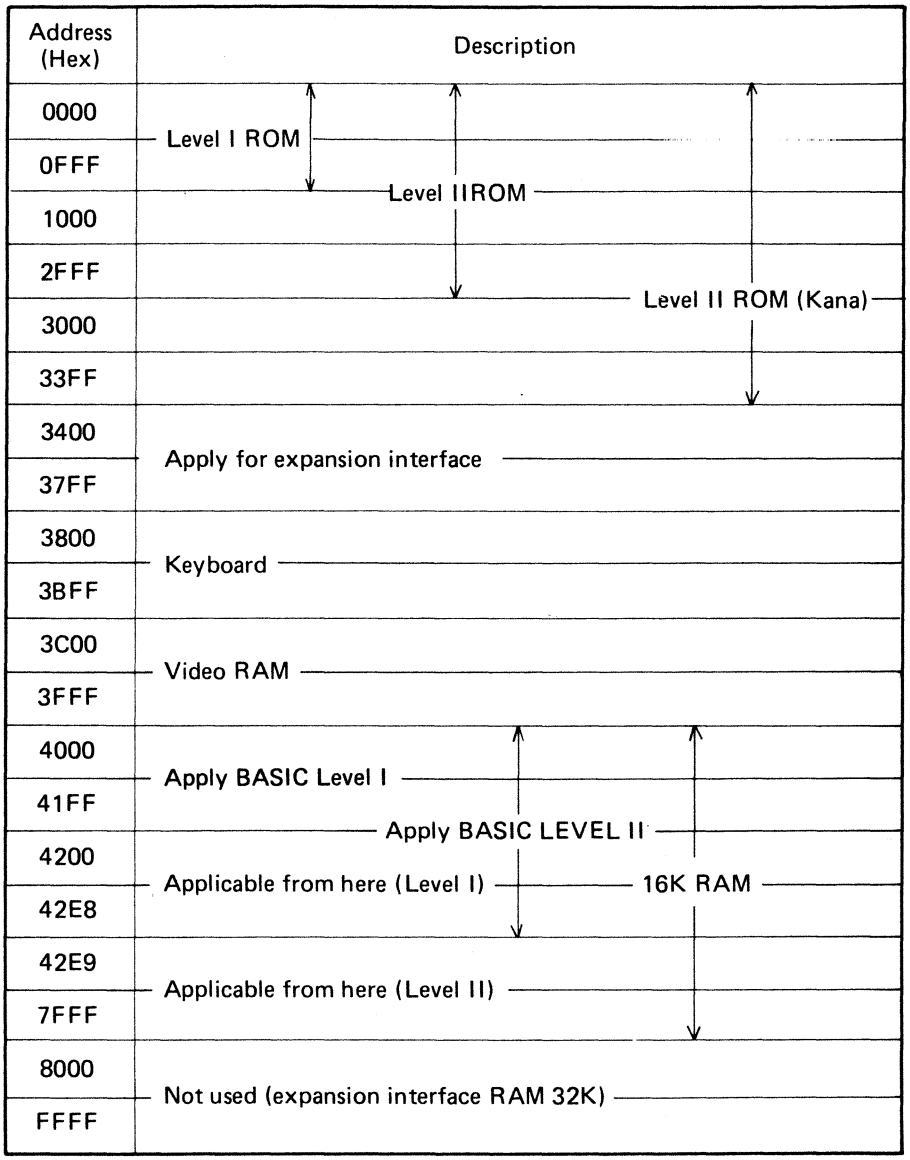


Figure 2-2. MEMORY MAP

3. PRODUCT SPECIFICATIONS

1. GENERAL

(1) Size

Width	Max. 423.5 mm (16.67")
Height	Max. 90.0 mm (3.54")
Depth	Max. 203.8 mm (8.02")

(2) Weight

2.1 kg (NET)

(3) Environmental

Operation	0°C (32°F) ~ 43°C (109°F) 40% ~ 80%
Storage	–40°C (–40°F) ~ 71°C (160°F) (no condensation)

(4) Line Noise

800 Vpp (Pulse width 1 μs)

(5) Static Discharge Immunity

2 KV C = 200 pF

2. SPECIFICATION

(1) Power Supply

5 Volt Line	D.C. 7.5 V (min) 1.4 A
12 Volt Line	D.C. 17 V (min) 360 mA

(2) Keyboard

ASCII + 10 Key	(65 Keys). . . . . .LEVEL I AND LEVEL II
FULLKEY + 10 Key	(66 Keys). . . . . .LEVEL II KANA
Software encoding	
Memory Map	3800 ~ 38FF

(3) Language

LEVEL I BASIC:	LEVEL I
LEVEL II BASIC:	LEVEL II AND LEVEL II KANA

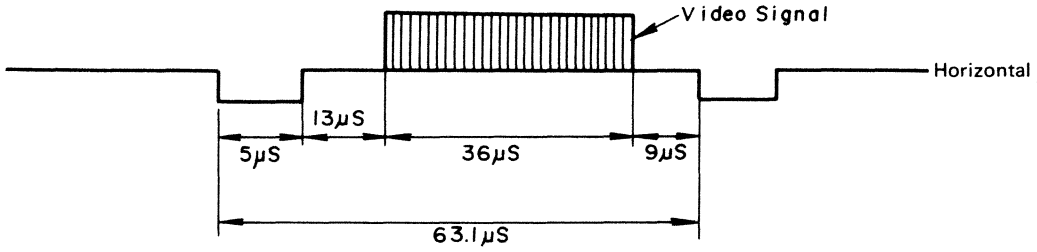
(4) Video (CRT)

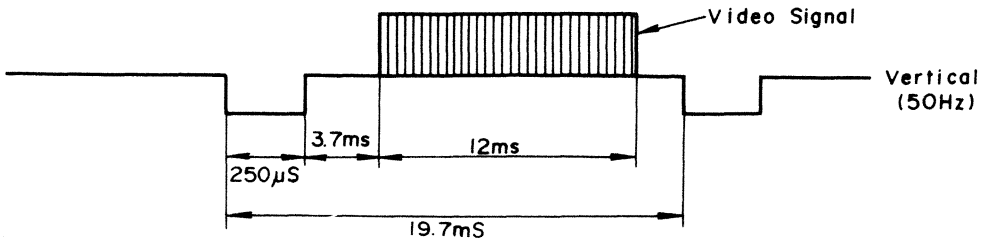
Video RAM . . . . . .1 KB

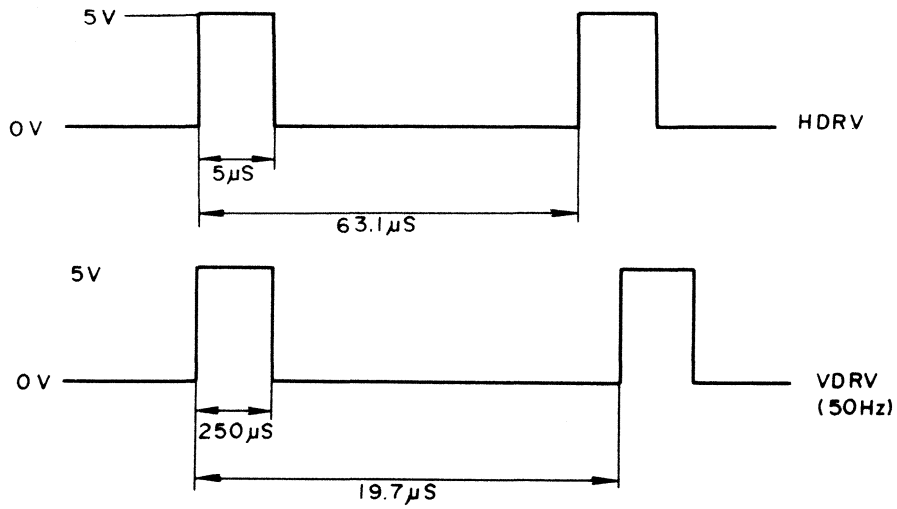
64 Character x 16 Lines or 32 Character x 16 Lines. . . .LEVEL II AND LEVEL II KANA

64 Character x 16 Lines . . . . . .LEVEL I

FONT	64 ASCII. . . . . .LEVEL I, II
	64 ASCII + 64 KANA . . . . . .LEVEL II KANA
	(Small Letter in Lower case: Option)
Graphic:	128 x 48 bit
Video Frequency:	50 Hz/60 Hz
Video Signal Voltage:	2 V
Blank Signal Voltage:	0.5 V
Sync Voltage:	0 V
Video Signal:	Composite Signal
Video Signal Timing:	







(5) Main Memory

ROM	4 K Byte	.....LEVEL I
	12 K Byte	.....LEVEL II
	14 K Byte	.....LEVEL II KANA
RAM	16 K Byte	

(6) CPU — μPD 780 (Z80)

(7) Clock Frequency — 10.6445 MHz

(8) Power Consumption — 21 Watts in Operation (CPU + CRT + CMT)

(9) LED

RED.....LEVEL I AND LEVEL II (power indication)

RED/GREEN.....LEVEL II KANA (Power indication and K/B mode indication)

4. THEORY OF OPERATION

The operation of TRS-80 is explained here with reference to the Schematic diagrams.

4-1. CPU and its Periphery

(1) Reset: The CPU reset at power-on is made by capacitor C70, ICs Z47, and Z46. These are connected to the CPU $\overline{\text{RESET}}$ terminals. The S2 reset switch is connected to CPU's $\overline{\text{NMI}}$ (Non-Maskable Interrupt) for use in resetting when CPU runs wild.

(2) System control lines: These consist of $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MREQ}}$, $\overline{\text{IOREQ}}$, and $\overline{\text{M1}}$. Z67gate converts these to signals RD*, WR*, OUT*, and IN*. Also with $\overline{\text{M1}}$ and $\overline{\text{JORQ}}$, signal INTAK* is made, and $\overline{\text{RD}}$, $\overline{\text{WR}}$, and $\overline{\text{MREQ}}$, signals RAS*, CAS*, and MUX are made up.

(3) Address buses: There are 16 (A0-A15) address buses from CPU, and through buffers Z49 and Z68, they connect to ROM and RAM.

(4) Data buses: There are 8 (C0-D7) data buses from CPU and through buffer Z23, they are connected to the various units. Address buses are single-directional bus lines but data buses are dual directional; so as the buffer IC, LS245 is used for data bus and LS244 for address bus.

(5) CPU: This is mostly covered in the outline description. In addition, μPD780 itself is provided with dynamic RAM refresh function. However, in this system $\overline{\text{RFSH}}$ terminal in CPU is not used but RAS* signal made by $\overline{\text{MREQ}}$ is used for refresh purpose. From $\overline{\text{MREQ}}$ terminal, address information for memory read or memory write is sent out on address bus. Also, when dynamic RAM refresh signal is sent out, signal for synchronization is also sent out. Refresh method by RAS* signal only is called RAS ONLY REFRESH.
CAS* and MUX signals are made by using CPU terminals $\overline{\text{RD}}$ and $\overline{\text{WR}}$. By taking the OR of the signals from $\overline{\text{RD}}$ and $\overline{\text{WR}}$, the output is sent into flip-flops Z62 and Z63 to make up the timing. This is indicated in Fig. 3-1. MUX becomes the select signal for Z13 and Z14 that perform the change-over between the row address and column address. Fig. 3-2 shows CPU Read/Write timing.

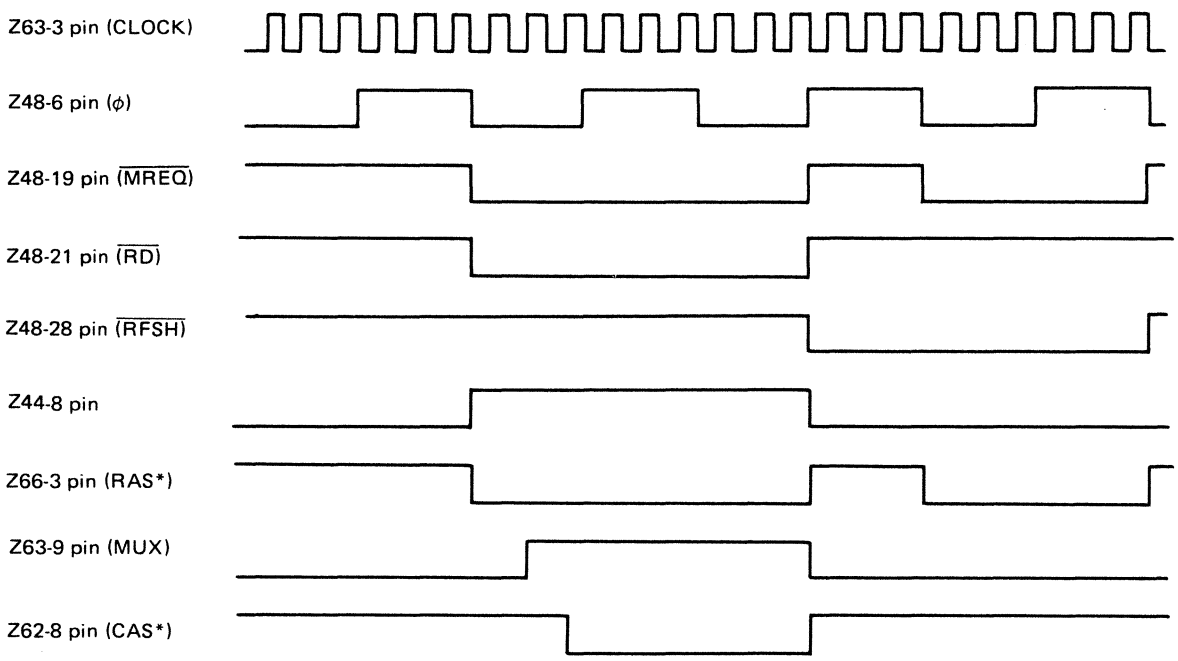


Figure 4-1 (a). DYNAMIC RAM CONTROL TIMING WAVEFORM (Instruction fetch cycle)

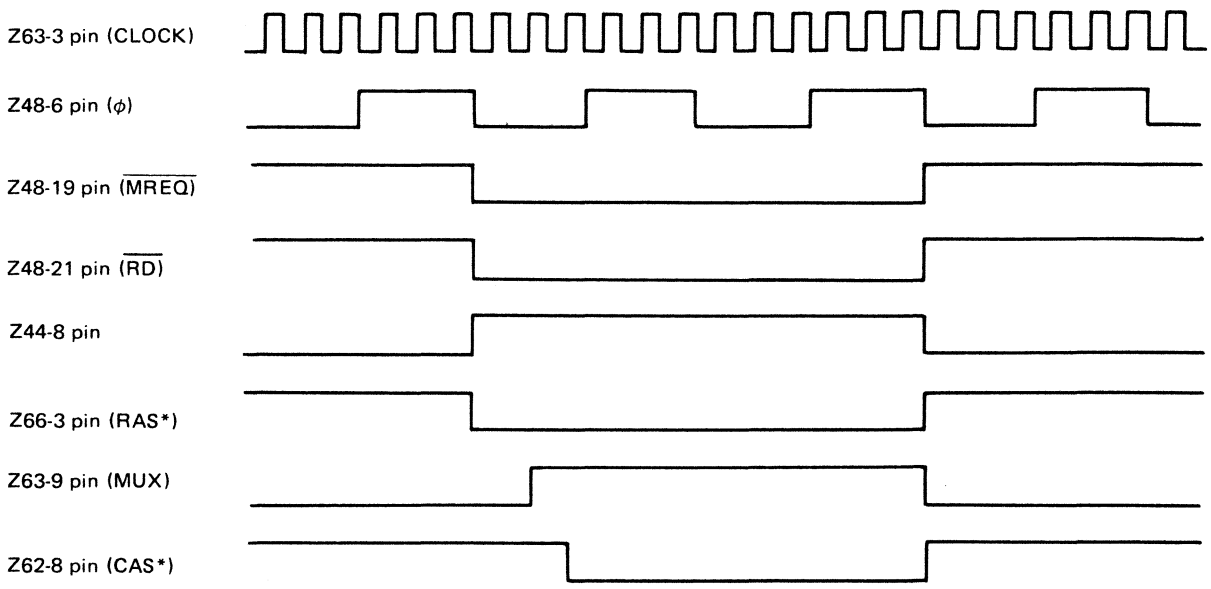


Figure 4-1 (b). DYNAMIC RAM CONTROL TIMING (Read cycle)

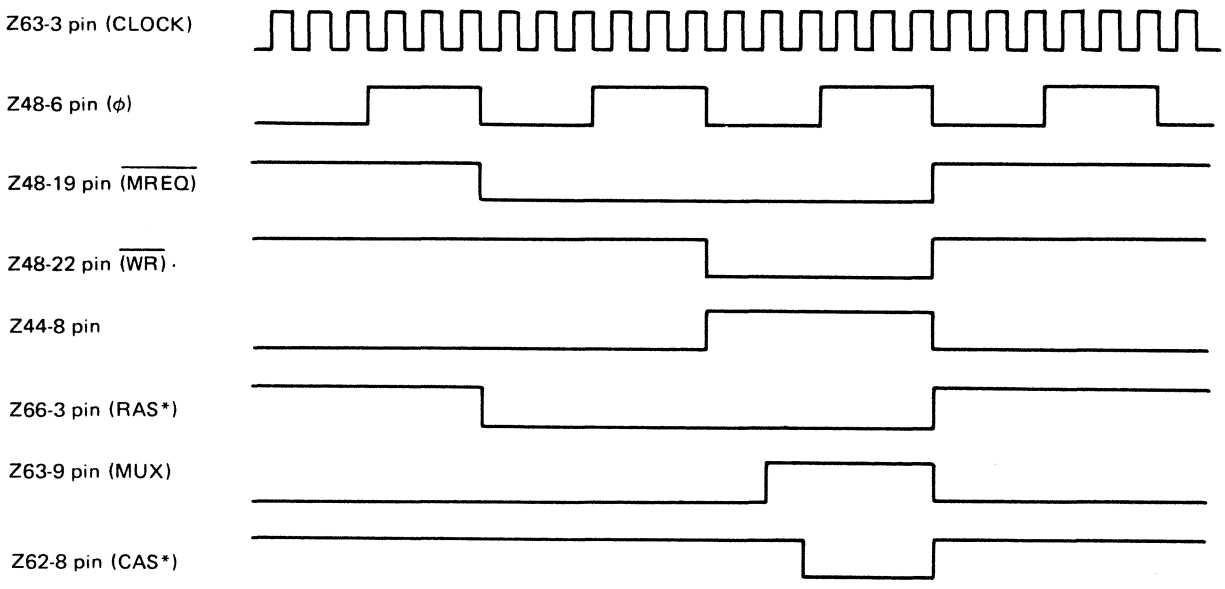


Figure 4-1 (c). DYNAMIC RAM CONTROL TIMING (Write cycle)

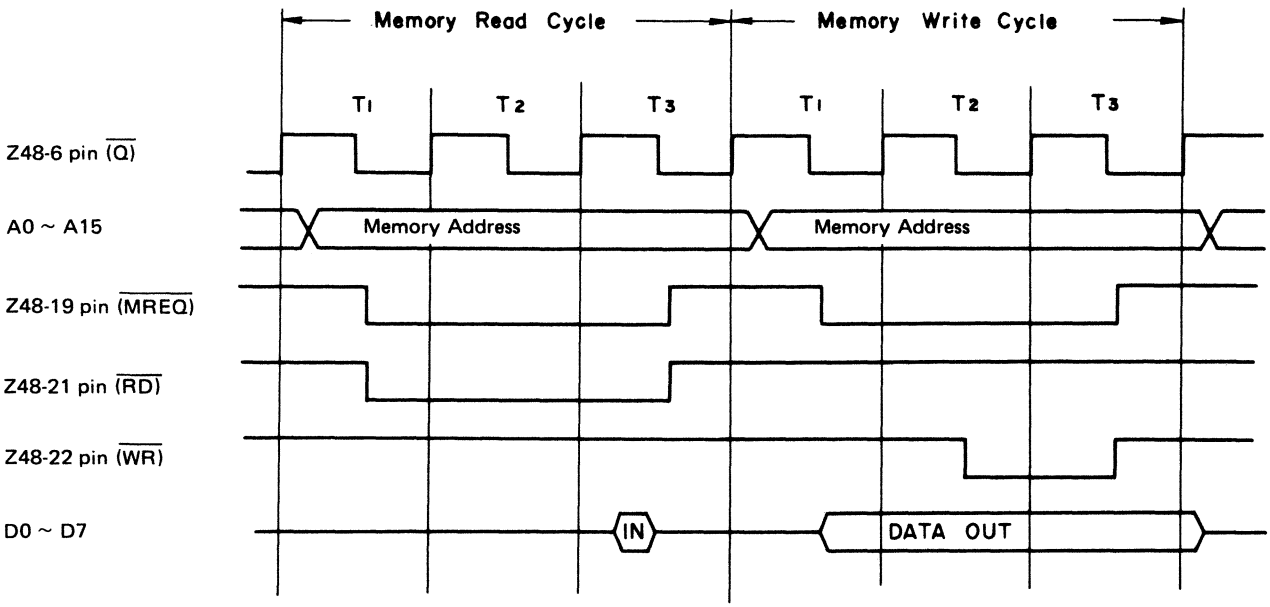


Figure 4-2. MEMORY READ/WRITE CYCLE

4-2. Address Decoder

The addresses are memory-mapped as indicated in Fig. 2-2. Due to this, the address decoder is required. The circuit diagram is shown in Fig. 4-3.

The following table shows how the addresses are designated in binary form.

	A15	A14	A13	A12	A11	A10	A9	A8	
From 0000	0	0	0	0	0	0	0	0	Level I ROM
To 0FFF	0	0	0	0	1	1	1	1	
From 3800	0	0	1	1	1	0	0	0	Keyboard
To 38FF	0	0	1	1	1	0	1	1	
From 3C00	0	0	1	1	1	1	0	0	Video RAM
To 3FFF	0	0	1	1	1	1	1	1	
From 4000	0	1	0	0	0	0	0	0	16K RAM
To 7FFF	0	1	1	1	1	1	1	1	

Z61 is a 2-input, 4-output decoder. A part of Z44 and a part of Z64, are also used. The decoder circuit is common to all Level I, Level II, and Level II Kana systems. The change-over is done by JP1, JP2, and JP3 connections.

	JP1	JP2	JP3
Level I	X	X	X
Level II	O	O	X
Level II Kana	O	O	O

Note

O: connection with jumper wire

X: no connection

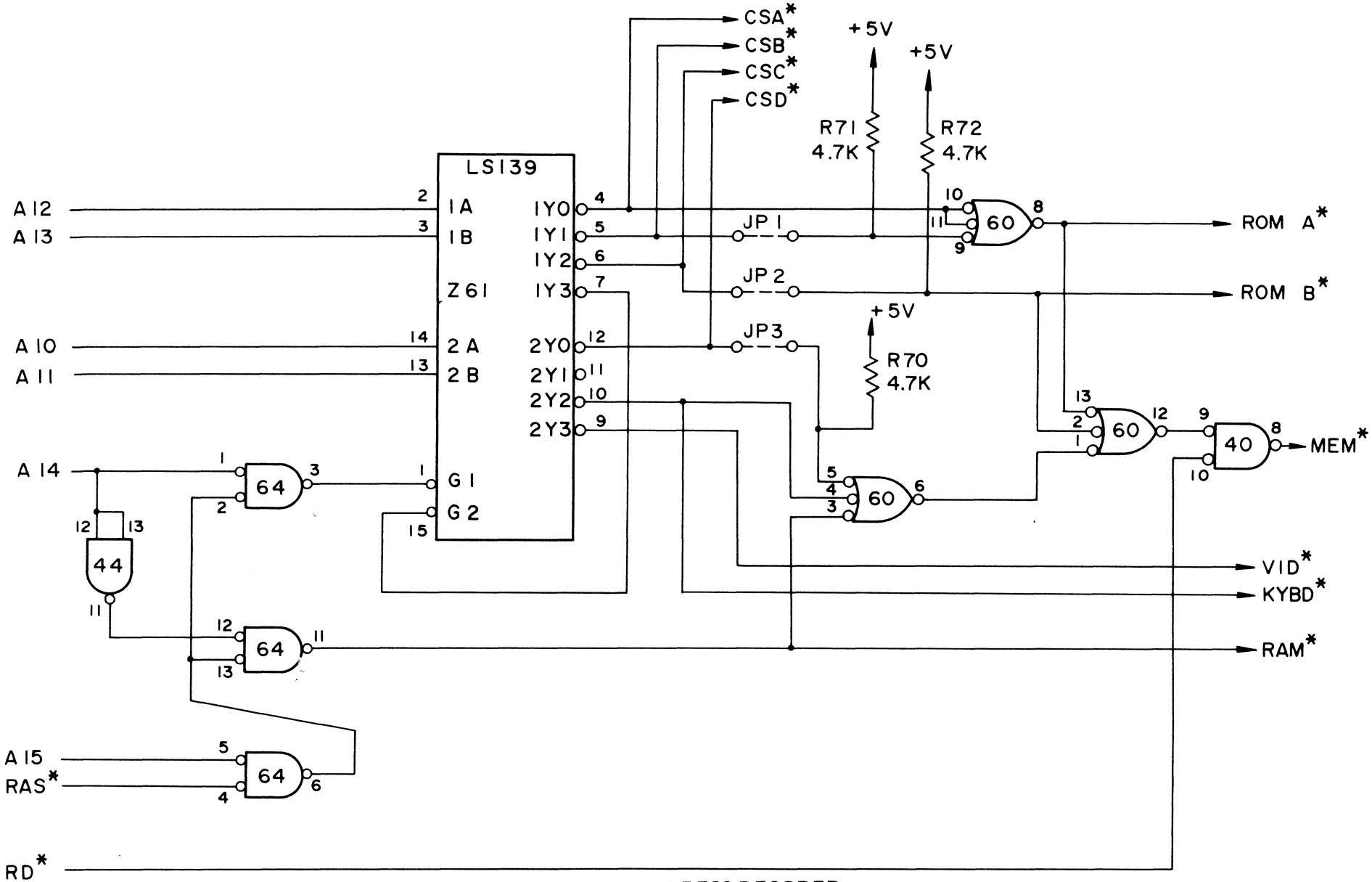


Figure 4-3. ADDRESS DECODER

With JP1-3 open, ROMA* signal selects Level I chip. When JP1 and 2 are shorted, ROMA* and ROMB* signals select Level II ASCII ROM chip. When all JP1-3 are shorted, CSA*, CSB*, CSC* and CSD* signals select Level II Kana ROM chip. When ROM and RAM send signal onto data buses, MEM* is the signal for opening the buffers attached to ROM and RAM outputs. RAM* signal is to control the MCAS* signal from dynamic RAM. VID* signal performs the change-over between the address signal to video RAM and the address signal from the counter making the video synchronizing signal, etc. KYBD* is the signal for opening the buffer for keyboard output.

4-3. ROM and RAM

The ROM and RAM have already been covered in Chap. 1 and 2, refer to these Chapters, too.There are three types of ROM, Level I, Level II, and Level II Kana. They have difference in capacity and contents. Level I ROM is 4K bytes, Level II ROM is 12K bytes (8K ROM and 4K ROM), and Level II Kana ROM is 13K bytes (4K ROM x 3 and 1K ROM).
RAM is 16K dynamic RAM consisting of 16K bits x 8 ea. Access time is 300 nS. Random read/write cycle is 510 nS and read/write is 575 nS. Refresh is made within 2 mS. Power supply is +12V, +5V and −5V. In TRS-80, +12V and −5V supplies are used only for the dynamic RAM. The two selectors, Z13 and Z14, in front of the RAM address input, make the change-over between the row and column addresses via the MUX signal. For the timings refer to Art. 3-1.

4-4. Basic Clock Generator

The oscillator circuit is made up of Y1 crystal oscillator, a part of Z50, and R56, R57, and C60. The output goes into pin 9 of Z50 and, after waveform shaping, the output comes from pin 8. This clock is used as CPU basic clock and also as CRT synchronizing signal. Z6 and Z27 make the basic signals for CRT synchronizing signal and CRT address and contorl signals. The MODESEL signal is to make the change-over in CRT regular display and double size display.

4-5. Video Synchronizing Signal Generator

To display on the CRT, the data in the video RAM must be changed over to signals for CRT. The video RAM address and CRT picture do not correspond to each other. Therefore, it is necessary to produce the address for the video signals. Also vertical and horizontal synchronizing signals are required. The circuit to produce these is explained here.
The display is normally 64 characters per line and 16 lines per display. By MODESEL signal can be changed to 32 characters per line. (In Level I Basic, only 64-character display can be made.)
This circuit for producing video signals is consists basically of the clock generator and the hex counters Z7, 28, 34 and 35. The main wave form oscillating circuit is made up of Z6 and Z65 duodecimal counters and Z27 multiplexer. The Z65 transforms the approximate 10 MHz pulse signal oscillated by the circuit to about 5 MHz (output from pin 12).
Fig. 4-4 and 4-5 show the timing charts. The double-size display condition is shown in Fig. 4-5.
The waveforms produced here decides the video RAM addresses and HDRV and VDRV for producing video signals, at the various stages of Z34, Z28, Z35, and Z7 IC's. Fig. 4-6 indicates the process for producing synchronizing signals.
The Z5 IC attached to Z28, Z35 and Z7 serve to reset the counters. Since Z28, Z35 and Z7 counters are non-synchronized, the NOT gate (in Z26) is provided for proper resetting.
JP6, JP7, JP8 and JP10 serve to change the vertical synchronizing signal frequency. Setting to 60 Hz is made by connecting between C~1. Setting to 50 Hz made by connecting between C~2. The purpose of this is to prevent the adverse effect of the magnetic field from power transformer by aligning the power frequency with CRT vertical synchronizing signal frequency.
The HDVR, VDRV, C2, C8, C16, L8, R1 and R2 signals oscillated from this circuit are combined with gates to produce the horizontal and vertical synchronizing signal timings. The horizontal and vertical synchronizing signals are mixed with Z32 to form the SYNC signal. This is mixed with Video signal and sent from J2 as output. The JP9 shown near the J2 connector in the circuit diagram is used only for Kana version destined for Japan; it is shorted for all others. This is due to the difference in CRT.

4-6. Video RAM, Character Generator and Periphery

There are two kinds of address signals for video RAM. One is the address signal to read data contained in the RAM or write data into RAM. The other is the address signal for read-out of data for video display. The change-over is performed by Z8, Z29 and Z36 multiplexers. For the video RAM, 1K byte (1K x 4 bits . . . . 2 ea.) static RAM is used. Since CRT picture displays 64 characters x 16 lines, a total of 10 address signals: C1, C2, C4, C8, C16, C32, R1, R2, R4 and R8 are sent out. C1, C2, C4, C8, C16 and C32 are used for the 64 characters and R1, R2, R4 and R8 are used for the 16 lines.
In the case of 64 characters x 16 lines, as the furthest left top end of the picture is addressed as line 0, column 0, the furthest right bottom end is addressed as line 15, column 63.

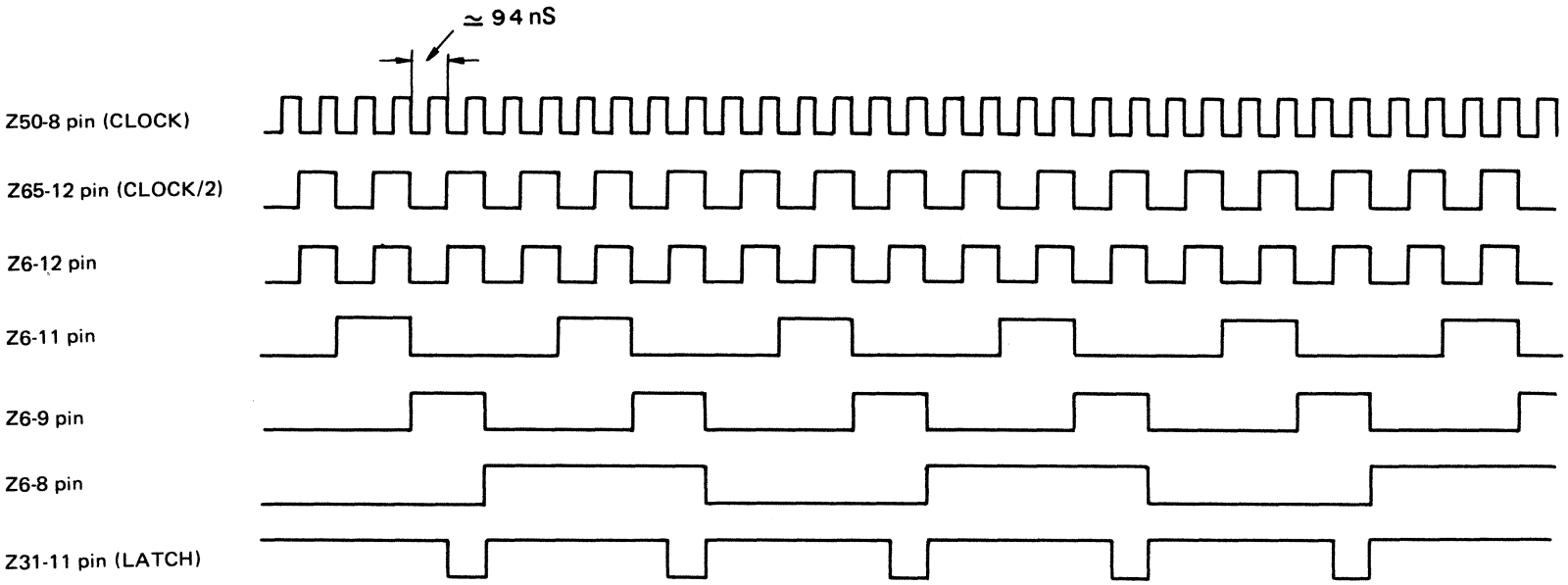


Figure 4-4. VIDEO PRODUCING CIRCUIT TIMING WAVEFORMS (64 characters x 16 lines)

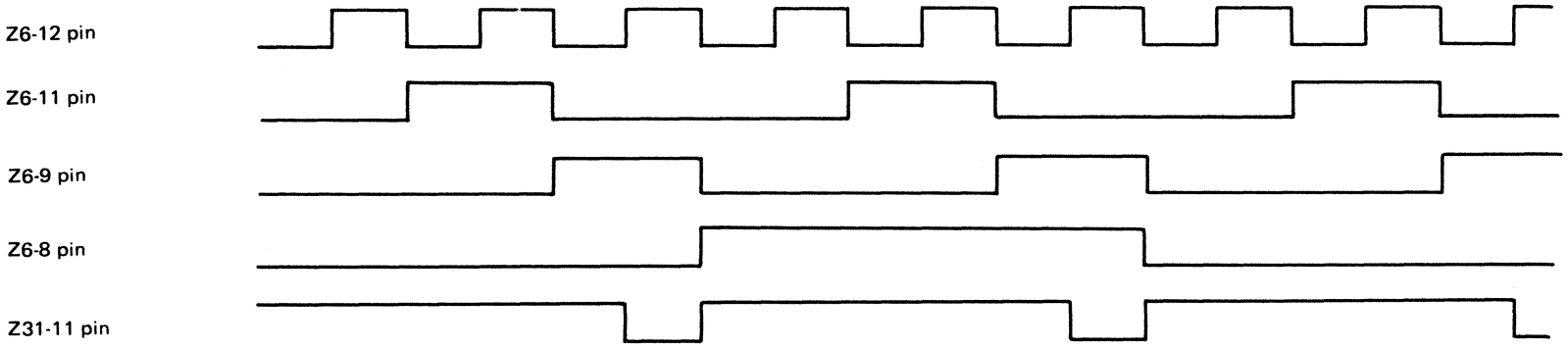


Figure 4-5. VIDEO PRODUCING CIRCUIT TIMING WAVEFORMS (32 charcters x 16 lines)

* Values within parentheses are for 50 Hz specifications (÷12/÷13) indicates that during one 50 Hz period, 21st becomes duodecimal counter and 5th becomes tridecimal counter.

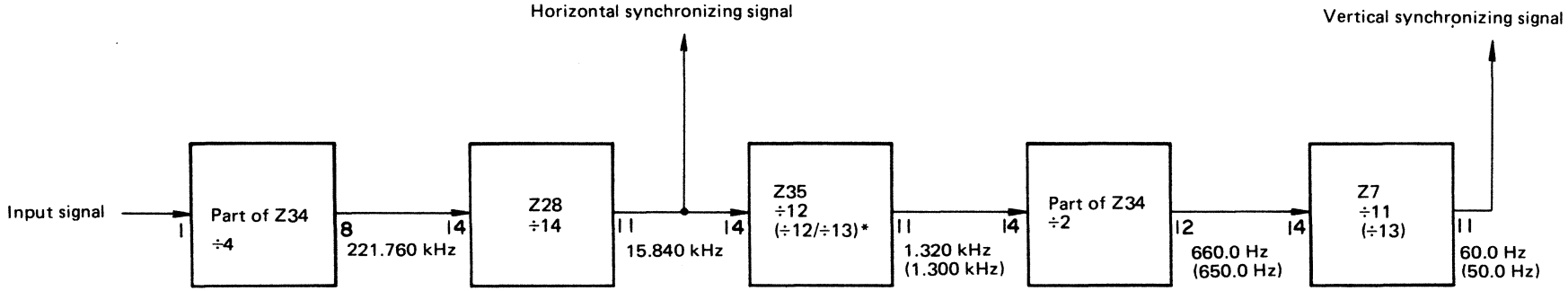


Figure 4-6. SYNCHRONIZING SIGNAL PRODUCING CIRCUIT BLOCK DIAGRAM

The video RAM is addressed in this way. The video RAM 3C00 indicates as line 0, column 0 and 3FFF as line 15, column 63. The entire picture consists of 16 lines, each line uses 12 scanning lines. Out of these, 7 scanning lines are utilized for actual display and the remaining 5 scanning lines used to provide space between the lines.
The Z35 in the synchronizing signal producing circuit is used to produce the scanning line for one character. The output from the counter L1, L2, L4 and L8 is utilized to produce the characters for one line. L1, L2 and L4 are sent to character generators RS1, RS2, and RS3 for selection of character pattern. L8 is used to provide the 5 scanning line distances.
The Z54 pin 1 output BLANK* signal provides the top, bottom, left, and right side blank spaces in CRT picture.
The Z12 is a buffer in video RAM data line. The direction in the video RAM data line and data line from CPU is changed as required for write-in or read-out of data, by CPU.
The Z11 latches the data from video RAM, and as timing (LATCH) signal is sent into pin 9 (CLK), sends out the data to character and graphic generators.
TRS-80 can select character or graphic display. As related already, characters are sent out from Z37 and Z38 character generators while graphics from Z39. The output signals are received by Z57 and Z58, and after serial conversion, they are sent out from pin 13. The change-over between characters and graphics at this time is performed by video RAM Z9 pin 11.
There are two character generators, Z37 and Z38. Z37 is for Level II Kana purpose, and Z38 for Level I ASCII and Level II ASCII purpose. The TRS-80 has space for only one of each (however, as option to Level II Kana, Z38 English small letter character generator can be mounted). Z53 flip-flop is located at end of chip select pin 17. By changing over JP4 and JP5, flip-flop output reverses to change the selected character generator.

4-7. Cassette Interface

The Z41 designates the cassette port addresses. When A0-A7 all become "1", "0" is sent out from Z41 pin 8. At this time, OUT* signal is sent out from Z30 pin 7, causing OUTSIG* signal to be sent out from Z41 output AND gate (pin 6). This signal is used for cassette control and video function control.
When Z41 output becomes "0", IN* signal comes in as input to Z40 pin 1 and INSIG* signal goes out as output. This signal is used only for Z59 control. Z59 input pin is connected to output pin of flip-flop actuated by Z31 NAND gate. When Z31 pin 10 becomes "0," pin 8 becomes "1" and the circuit connected to this flip-flop goes into set state.
This Z31 flip-flop becomes reset when OUTSIG* becomes "0." Under control by INSIG*, Z59 checks the state of Z40.
When CSAVE function is started, cassette motor should start turning. CPU makes the OUTSIG* "0" and has D2 send out "1". When OUTSIG* changes from "0" to "1", D2 signal "1" is sent out to Z4 pin 2, causing signal to be set to Z3 relay driver. Z3 pin 5 drops to "0", causing current to flow into relay coil K1 and close K1 points. This results in connector J3 pins 1 and 3 to contact and start turning the cassette recorder motor wired to this connector.
When the motor starts turning, the signal to be recorded on the tape is sent out form CPU. The timing signals for performing the recording are all made for control by software.
Z4 receives the output from CPU and composes the output signal. This output is called CASSOUT and the waveform is shown in Fig. 4-7. This waveform is combination of outputs form Z4 pins 11 and 15.
In Fig. 4-7, the interval from one bit to the next bit is about 4 mS in Level I and about 2 mS in Level II. Whether the signal is "0" or "1" will depend on the presence of the signal between these bits.
When data is sent out from CPU, it is done as follows.
When CSAVE starts, "0" bit is sent from Z4 for about 2 sec. Next, code A5 is sent out to synchronize CLOAD. After this, the necessary data is sent out.

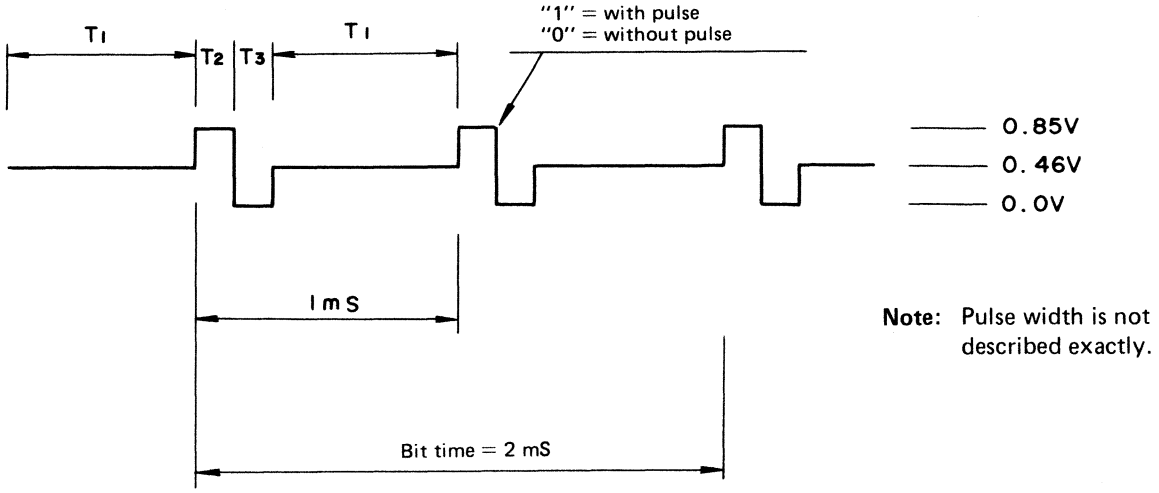


Figure 4-7. CASSOUT WAVEFORM

In the case of CLOAD cassette audio signal (CASSIN) is attained from connector J3 pin 4. This signal passes through resistor and capacitor, and enters into Z25 operational amplifier. The processing of the audio input signal is shown in Fig. 4-8.
When the CLOAD command is entered in from the keyboard, OUTSIG* signal becomes "0," to start moving the cassette recorder, and at same time, reset the Z31 flip-flop. When the first bit arrives, Z31 pin 10 becomes "0," causing the flip-flop to set.
Fig. 4-9 shows the above data latch timing. The INSIG* and OUTSIG* signals are controlled by the software in the ROM.

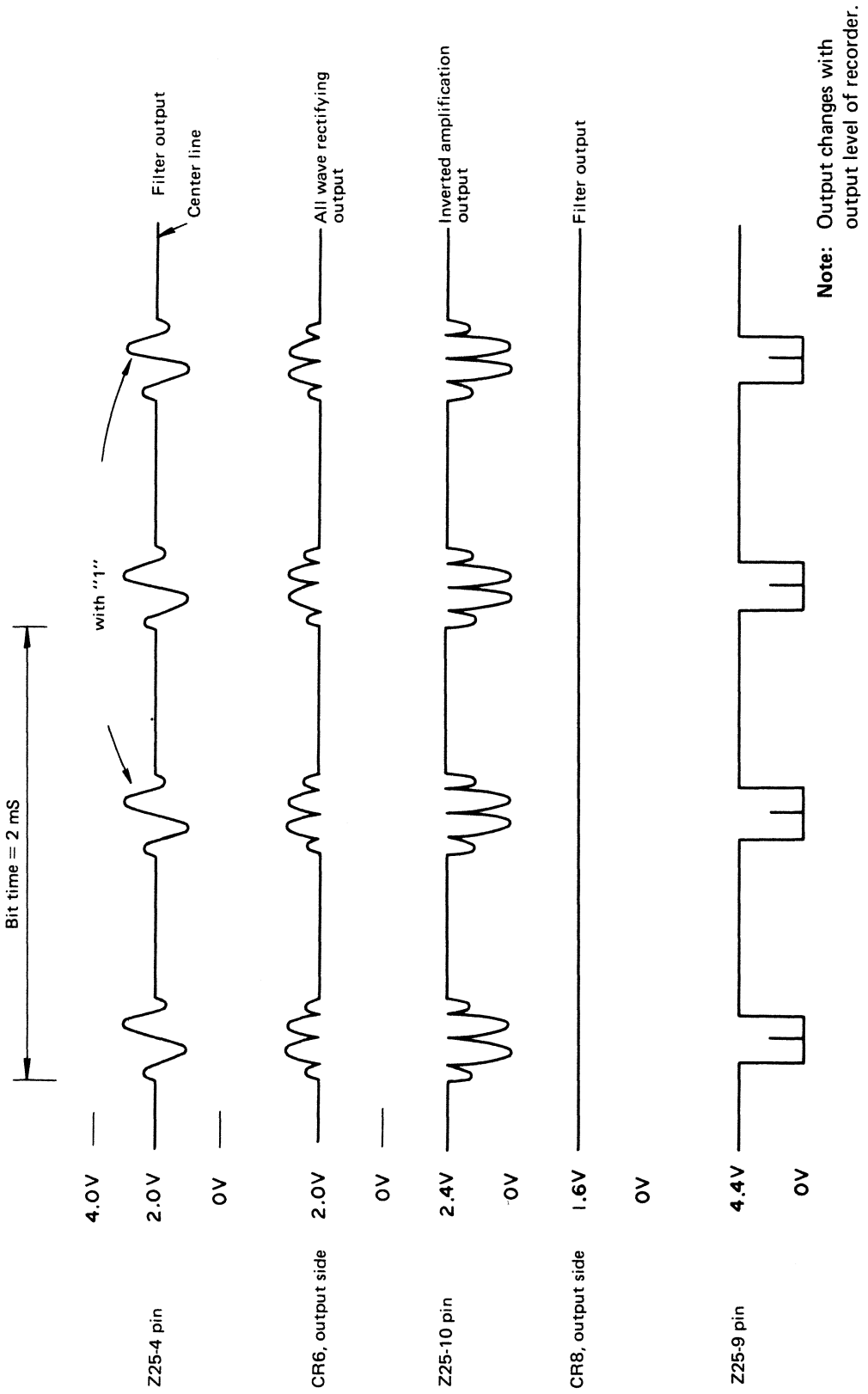
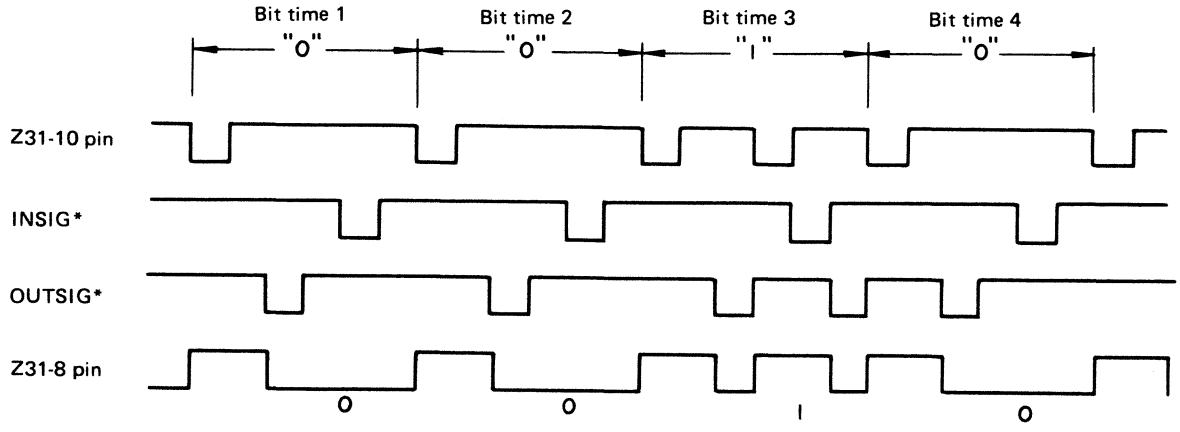


Figure 4-8. AUDIO INPUT SIGNAL PROCESSING



Note: Pulse width is not described exactly.

Figure 4-9. DATA LATCH TIMING

The CPU checks the condition of Z31 pin 10 by impressing INSIG*. Since Z31 pin 8 is "0" at bit time 1, this shows that data is "0". The flip-flop is set at start of bit 2 and reset by OUTSIG*. When check ismade through Z59 by INSIG*, it shows again that data is "0" so that CPU determines "0."
When check is made with INSIG* at bit ime 3, the result becomes "1" so CPU sends out OUTSIG* to reset the flip-flop. At bit time 4, "0" is read out again.

4-8. Keyboard

TRS-80 keyboard consists of 65 single-pole switches (66 for Level II Kana) mounted on printing board. These are normally open keys and actuate only when the keys are pressed.
In this keyboard system, the keys are arranged in matrix form. The ROM software detects which key has been pressed and the CPU makes the conversion to ASCII code corresponding to the key pressed.
Keyboard selection is made in accordance with decoder output KYBD*. When this signal is "0", Z3 and Z4 (Z8 in Kana keyboard) will be in operating state but when key is not pressed, the input will pass through 4.7 K resistor and connect to +5 V.
Then when any key is pressed, address line state is transmitted to the data line. For example, when A0 is at potential "1," the top horizontal line in the key matrix will be at "0". If the A key is pressed at this time, the second vertical line from the left will become "0." When the KYBD* signal becomes "0," the fact that A key has been pressed will be transmitted through MD1 to CPU.
In the above manner, CPU checks whether any key has been pressed by varying each address line signal.
In addition, CPU checks whether the shift key has been pressed and makes the conversion to the corresponding ASCII code.
A point to be noted here is that open collector ICs are used for Z1 and Z2 (Z2 and Z3 in Kana keyboard). Thus, there will be no problem even if two or more keys are pressed simultaneously.

4-9. Power Supply

The following three kinds of power are required in TRS-80.
a) +12 V, 360 mA
b) +5 V, 1.4 A
c) −5V, 1 mA
The +12 V and −5 V are required only by system RAM and everything else needs the +5 V power. The +12 V and +5 V are stabilized power and moreover, their outputs should be protected against shorts. The −5 V is not as critical as the above two and uses Zener diode for regulation.
The +12 V input power supply is rectified but not stabilized. Turning on the S1 switch will impress voltage of around 20 to 30 volts on C9, Q6 and Z2 pin 12. The pin 12 input is impressed on the Zener diode Za to allow fixed current to flow. Zener voltage of about 7.15 V goes out form Z2 pin 6 as output.

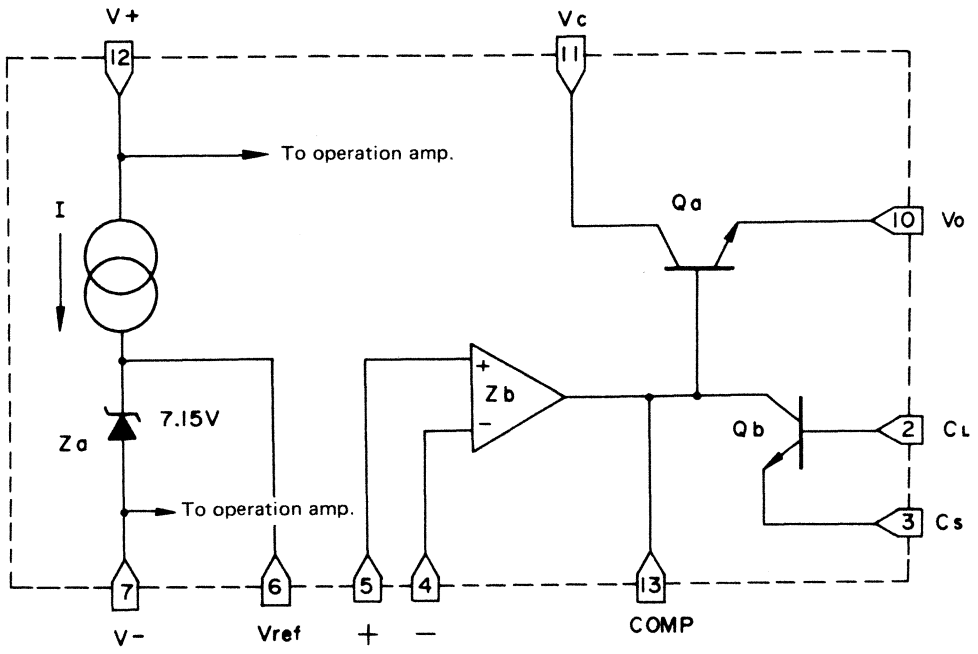


Figure 4-10. 723 REGULATOR BLOCK DIAGRAM

Fig. 4-10 indicates Z1 and Z2 regulator purpose IC's in model form. Pin 6 is connected to pin 5 through R22. This becomes the input to + side of operational amplifier indicated by Zb.

The input to − side of the operational amplifier connects to the adjust terminal of variable resistor R23 and produces +12 V stabilized voltage by R23, R25 and R26 resistor network.

R30 is a resistor for current control. In Fig. 4-10, the Qb transistor serves to protect the Q6 transistor. The capacitor connected to pin 13 serves to compensate the frequency and prevent the operational amplifier from oscillation.

The 723C stable voltage regulator is also employed in +5 V power supply. In principle, it is practically the same as that for +12 V. In the 5 V power supply, AC 17 V is impressed on CR1 and after full-wave rectification, about 10 V is impressed on both ends of C10.

The power to Z1 is taken from R30 side of 12 V power supply. The Zener voltage 7.15 V output from pin 6 is divided by R18, R17 and R24 resistors and impressed on + side of operational amplifier and adjusted to 5 V by R17.

Q3 is used to control the large current from Q4. From the Q4 collector, the current is passed through current limiting resistor R16 and supplied as 5 V. The Q5 transistor performs current control surveillance.

C11 performs the same work as C16. C12 and C13 are output filters. In addition, 33 capacitors each 0.1 μF are employed as by-pass capacitors to suppress noise and installed at various parts of the printed circuit board. CR2 serves to protect the TTL elements from damage in case the 5 V line should short with other power supply.

Unless the +12 V power supply operates normally, the +5 V power supply will not work accurately so that in case of adjustments, adjust the 12 V power accurately first and then perform the adjustment of +5 V power.

The −5 V power supply is only for small current flow. It takes the voltage from CR1 − side terminal with about −11 V voltage impressed on both C5 terminals. This voltage passes through R12 and stabilized to 5.1 V by Zener diode CR3.

5. TRS-80 ADJUSTEMENTS AND TROUBLESHOOTING

5-1. Disassembly Method

(1) Position the TRS-80 main body, keyboard down, on a soft surface.
(2) Remove the six screws from the bottom of the case. There are three different lengths of screws, consisting of two each. When reassembling, make sure not to intermix the different length screws.
(3) Position the keyboard up and carefully separate the case upper half. At this time, be careful not to lose the two long spacers inserted between the case upper half and keyboard.
(4) After laying aside the case upper half and the long spacers, carefully lift up the keyboard from the case lower half. Use care at this time not to place excessive force on the connection cable.
(5) There are six spacers between the two printed circuit boards. Remove these and set them aside, and use care to see that they do not get lost.
(6) Remove the two printed circuit boards by lifting them up from the case. Use sufficient care not to strain the connection cable.
(7) Arrange the two printed circuit board to facilitate the operations and such that the cable will not be strained. If necessary, the two printed circuit boards can be separated into single boards by removing the connection cable from the connector.

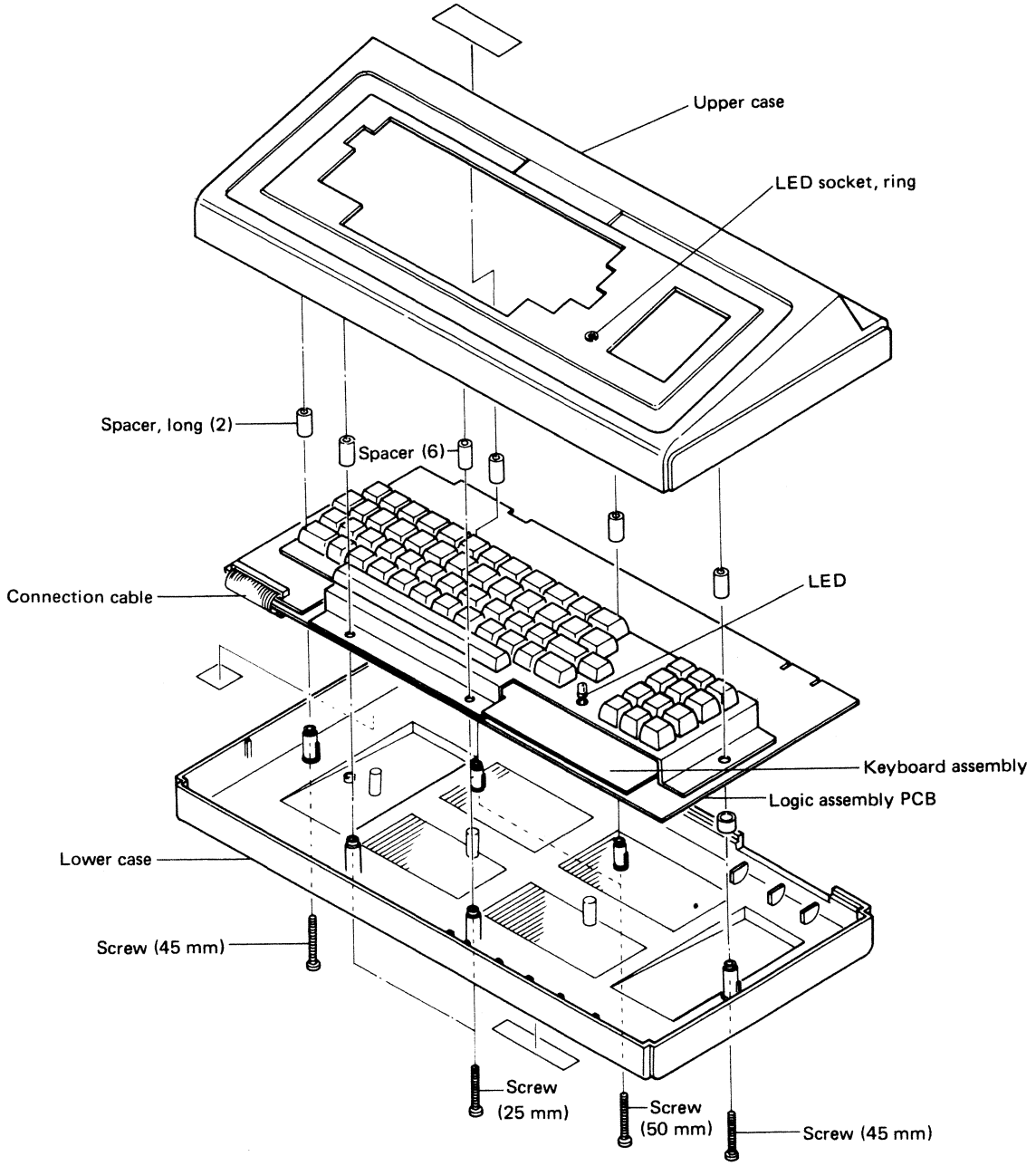


Figure 5-1. TRS-80 DISASSMBLY METHOD

5-2. Power Supply Checks and Adjustments

After removing the printed circuit boards from the case, connect the power and the video connector plugs.

CAUTION

When the keyboard printed board is laid in normal position, the CPU printed board exposed surface will be reverse to that when assembled in case. Be sure to connect the power connector J1 and tape recorder connector J3 to correct places. The J1 connector is the one nearest to the power switch.

Turn on the CPU printed circuit board switch and CRT power switch. Whether anything will be seen on the display will depend on the type of the trouble.
First of all, make the power supply voltage test (refer to Fig. 5-2).

(1) Connect the – side of the digital voltmeter (Use DC range) or circuit tester to the check terminal GND. Some printed circuit boards are not provided with check terminals, so in such case, make the connection to one end of the capacitor C10. This C10 is the largest capacitor on the printed circuit board.

(2) Measure the voltage of the +12 V power supply at +12 V check terminal. The voltage at this terminal should be 12.0 V (11.4~12.6 V). If the voltage is not within these limits, adjust R23 for correct value. On printed circuit board not provided with check terminal, check the voltage at the terminal at outer edge of printed circuit board nearest to R30.

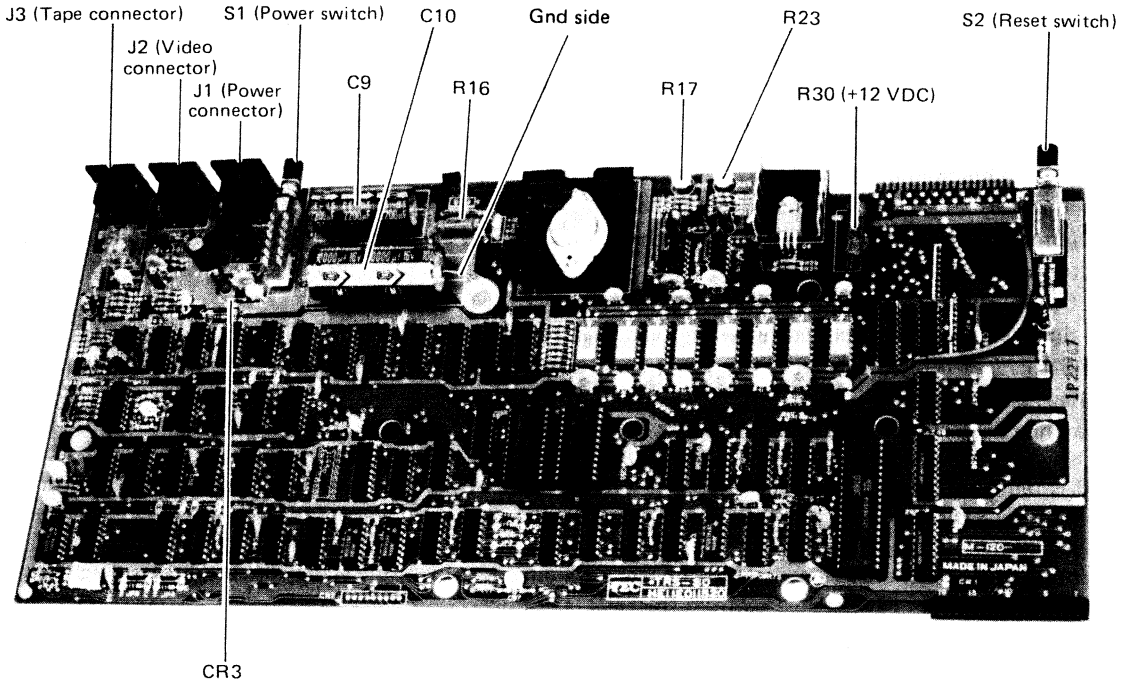


Figure 5-2. LOGIC ASSEMBLY PRINTED CIRCUIT BOARD

(3) Measure the voltage of the +5 V power supply at +5 V check terminal. This voltage should be 5 V (4.75~5.25 V). If the voltage does not fall with in this range, adjust R17 for correct value. For printed circuit boards not provided with check terminal, check the voltage at the terminal at left outer side of R16 on printed circuit board. This R16 is a 2 W resistor located between the two large capacitors C9 and C10.
Do not make the 5 V voltage adjustment until the 12 V voltage adjustment has been completed.

(4) Measure the voltage of the −5 V power supply at −5 V check terminal. This voltage should be −5 V (−4.80 ~ −5.50 V). This voltage cannot be adjusted. If the voltage fails to fall within the limits, check for defective parts and make replacements.
For the printed boards equipped with check terminals, the distance between check pins is narrow so use care not to short them when adjusting power voltage. If shorted, there will be danger of damaging the power supply and IC elements.

5-3. Trouble Detection Procedure

Troubles appear in many forms and different symptoms are indicated depending on the kind of trouble. For example, when the power is turned on, meaningless characters and graphics could fill up the entire display.
This is one of the worst kind of troubles. Normally, when the power is switched on, the CPU will immediately perform the program for initialization. When such a meaningless display is made, that means the program for initialization has not been realized.
In such a case, where would the cause of trouble be hidden? It could be in the ROM, RAM, or in the CPU. The trouble could also be due to loose solder or short-circuit at some place. There would be numerous causes that could be thought of.
Such being the case, when a trouble develops, where would be the best place to start working? The following are the procedures for locating the cause of trouble.

(1) Section trouble detecting method

Fig. 5-3 indicates a method of checking for troubles by removing the parts and finding out at what section the trouble would be.
The trouble mentioned above, the meaningless character and graphic pattern with the power on, is explained here. Refer to the Flow Chart block 1.
In block 2, the power cable and video cable are disconnected once and then reconnected.
Block 3 is for indicating the decision. It decides whether the operation in block 2 will still allow meaningless display or will correct it.
If the display returns to normal, block 4 will indicate that cable connection is defective or about to become open, or the poor soldering on cable connection. In such case, check for improper cable connection. It could also be a simple case of cable and connector not being properly connected.
In block 5, the power switch is turned off and then turned on after 10 sec.
This is the time required for the logic circuit to restore normal initialization. If in block 6, "READY" is indicated at Level I and "MEM SIZE?" or MEMORY SIZE?" at Level II or Level II Kana, move to block 7. At this time, parts like switch S2 or C70 could have been defective.
If the display had been meaningless in block 6, move to block 8.
In block 8, the ROM is removed. **Power must always be switched off before removing the ROM.**
When ROM is removed, no program can be sent to CPU. On the display, @ 9 will fill the screen in 64 charactor mode or in 32 character mode either @ or 9 will be indicated, and VID* will be sent continuously. There will be flickering at this time. (In the case of Level II Kana, ¥is indicated instead of @).
If @ 9 cannot be seen or can only be seen partially, the problem could be in the synchronous generating circuit or video RAM.
If the display here is also in meaningless pattern, the CPU is not operating properly.
The flow chart here indicates only a procedure. It does not necessarily mean that you can shoot the trouble cause automatically.
For example, in block 11, several @ 9's on the display is not always due to synchronous generating circuit malfunctioning.
The Fig. 5-3 flow chart is not an absolute thing. It merely indicates one of the courses for troubleshooting.

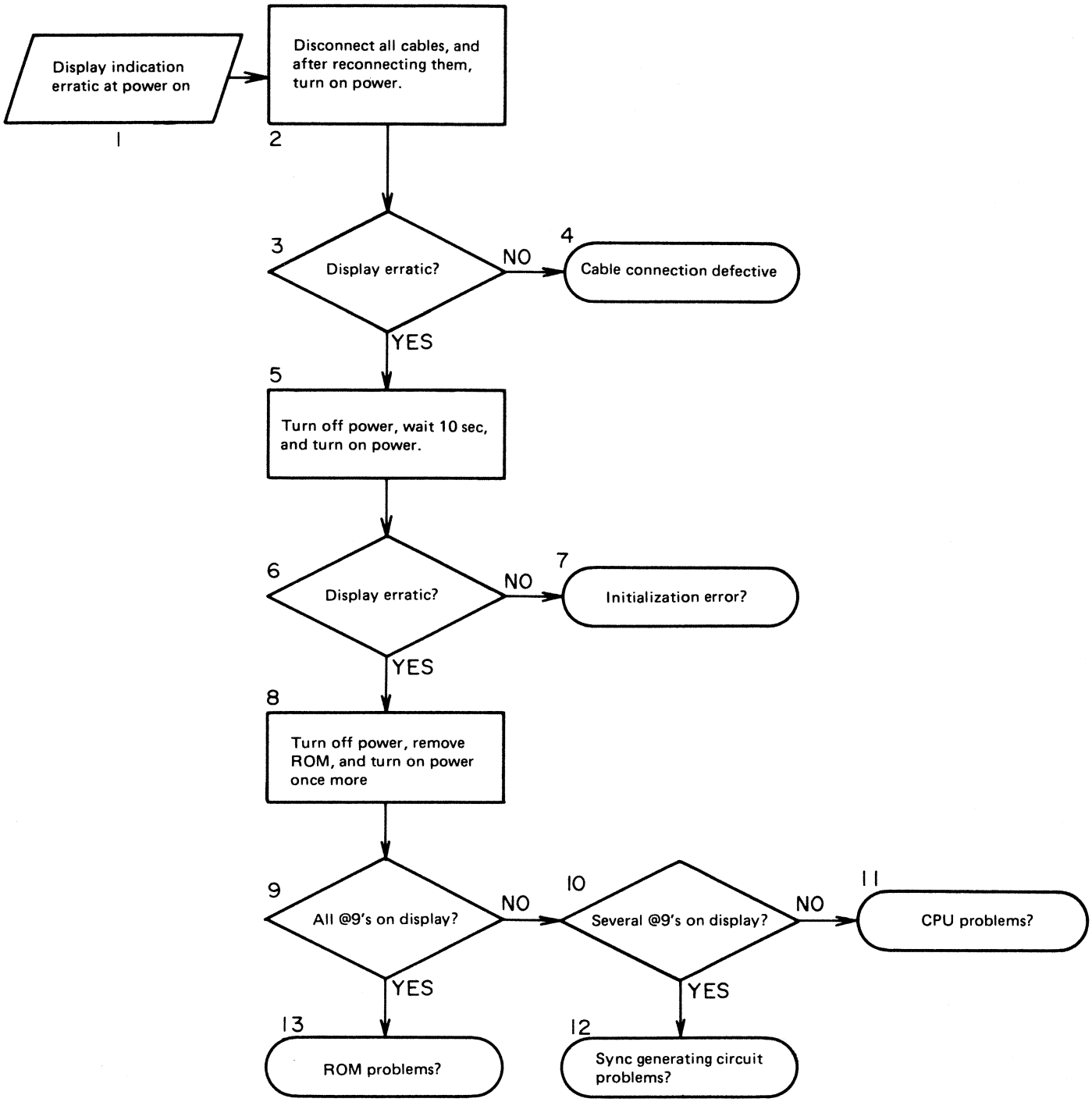


Figure 5-3. FLOWCHART FOR TROUBLESHOOTING

(2) Signal status

As a method for detecting defective place, first find out if wrong signal is being sent out from any of the places, and then trace the wrong-value signal. When you come to a place where normal signal is sent out, the faulty place is between the wrong and correct signals.

(3) CPU

Faults in the CPU, μPD780 (Z80), are difficult to handle. They appear as faults in the address and data buses or buffers or as wrong CAS/RAS timing. In this event, what must be done first is to replace the CPU because it can be easily removed from the socket. The trouble may be originated outside the CPU, but CPU replacement is the first step to do.

The procedure for troubleshooting the CPU is flowcharted in Fig. 5.4. At left on the flowchart are questions about signals. Start with these questions, and proceed to the right if the signal is abnormal.

Fig. 5-4 indicates a flowchart for trouble diagnosis relating to CPU. This flowchart indicates the procedures for checking the CPU when it had been judged faulty. In this flowchart, the check flow of the main signals are shown at the extreme left side.

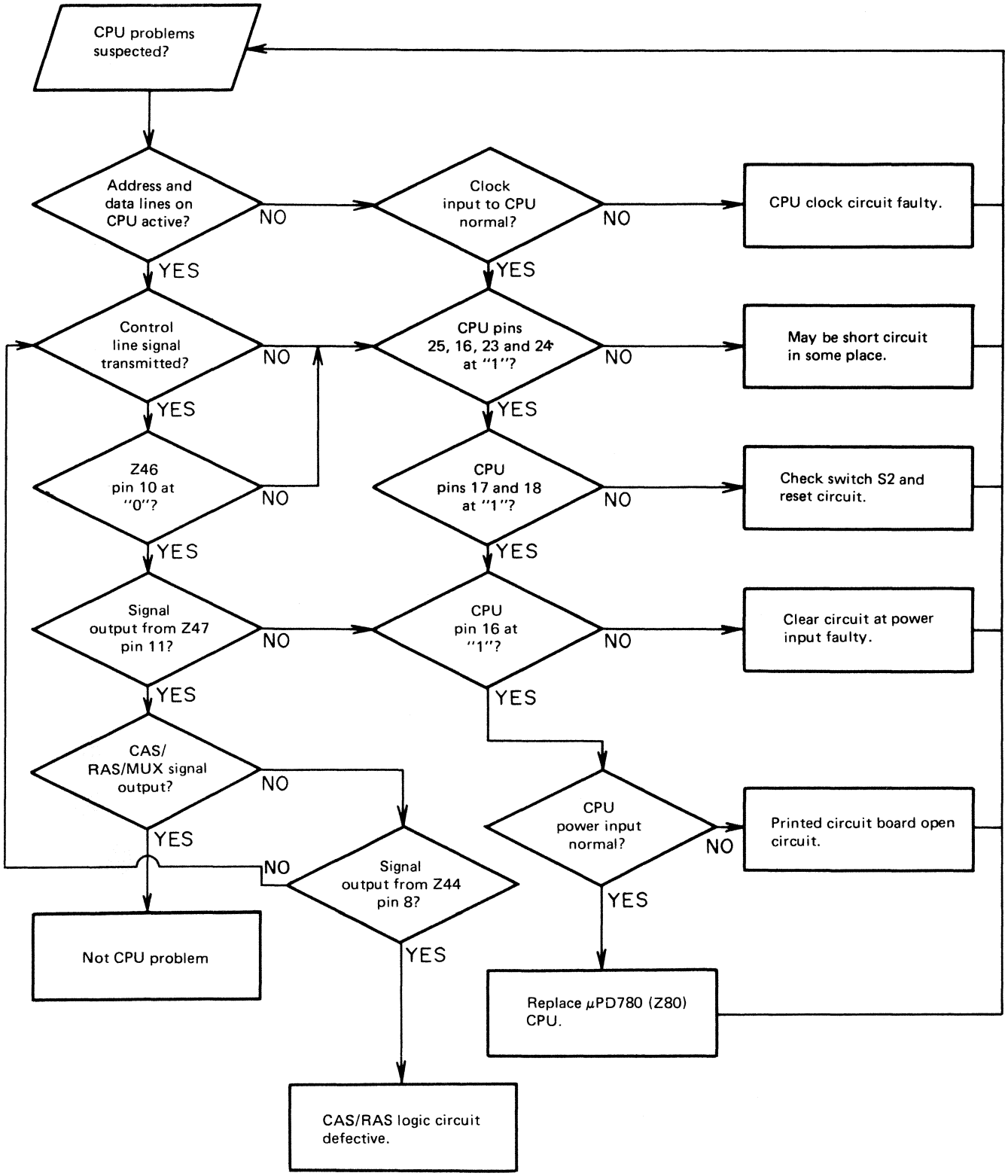


Figure 5-4. CPU TROUBLE DIAGNOSIS FLOWCHART

First of all, check the CPU address and data lines to see if the pulse signals are being sent out. If pulse signals are not being sent out over these lines, the trouble would be in the CPU clock pulse input circuit.
The address and data lines from the CPU are parallel lines in close proximity on the printed circuit board. If the address lines should develop mutual shorting, floating signal level could be indicated.
To check if shorted, set the CPU pin 25 or R55 terminal to 0 volt. By doing this, CPU side address line will be at floating signal level and address buffer will also become floating.
In the case of data lines, even when in normal state, they could become at floating signal level, and could take logic 1 or logic 0 value, making it fairly difficult to determine if shorted.
Even when the TEST* signal is made logic 0, data lines cannot be disconnected from CPU like the address lines. To check if the data line is shorted, first pull out the CPU from its socket and set the $\overline{RD}$ terminal (pin 21) to logic 1. Then try impressing TTL level signal on Z23 terminal on input side from CPU. Use the signal sent out by synchronizing signal generating circuit, as the signal for this purpose.
This signal sent in will appear at the corresponding output side. If it does not appear on any other data lines, the condition is normal. If this input signal appears on any of other data line, that line is shorted with the corresponding line.

(4) ROM

Problems associated with ROM can be classified into three areas.

Address circuit
Data circuit
Chip select circuit

The following covers the matters on which problems are likely to occur.

(i) Address circuit
The address circuit lines are laid parallel in close proximity so that shorts could develop. Also there may be defective contact with sockets and open circuits. There are cases of ROM having been partially jarred out from its socket by shocks. The address lines should be checked at the ROM terminals. One-pulse signals normally flow through the address lines. When the TEST* is made 0 volt at CPU, the address lines will be cut off from CPU, to enable making short and open circuit tests on the address lines.

(ii) Data circuit
There are two causes for problems arising in the data circuit. One of them is the ROM bit having become bad, for which there is no repair method. Replace the ROM.
The second is short or open circuit in the data lines. For this, check the data line at the ROM pins with circuit tester.

(iii) Chip select circuit
Signals associated with chip select are ROMA*, ROMB*, CSA*, CSB*, CSC*, CSD* and MEM*. ROMA* is used by ROM chip select at Level I, ROMA* and ROMB* at Level II, and CSA*, CSB*, CSC* and CSD* at Level II Kana. MEM* controls the data line buffers (Z24 and Z30) at RAM/ROM read out. Check the JP1–JP3 for proper connection, the chip select signal lines for short or broken pattern, and the Z61 input and output for proper correspondence. If the address lines are not in proper state, Z61 will not function correctly.

(5) RAM

CAUTION

When handling the RAM's, be very careful not to damage them by static discharge.
Before touching the RAM's, get rid of your own static electricity by touching nearby ground. This could be done by touching the negative-side terminal of C10 capacitor.
When moving the RAM from one place to another, use a mat impregnated with conductive paint. Never use white styrofoam. This can generate extremely high static voltage capable of damaging the RAM.
Also do not use cellophane tape to hold the RAM's in sets. The high voltage will be produced when removing the tape.

The ROM can still read/write or addresses can be changed over even it is defective.
Check the RAM power supply pins to see if power is being supplied properly to RAM. Pin 1 is –5 V, pin 8 is +12 V, pin 9 is +5 V, and pin 16 is GND.
Check to see if RAS and CAS signals are being impressed and if the WR* signal is coming in. Check the MUX signal entering into pin 1 of Z13 and Z14 multiplexers to see if functioning properly. Also check the pin 15 on the same IC's is at logic "0".
Check the address signals to see if entering properly into the RAM's and also if the MEM* signal is sent out from Z40 pin 8.
If the RAM is judged to be defective after making the above check up, replace the RAM. Try replacing RAM one by one when you can't identify which RAM is defective.

(6) Address Decoder

When the address decoder becomes defective, the different memories will not function. For example, if the RAMs fail to operate at all, RAM* signals may not be coming out.

Thus, if any of the memories fail to operate consistently, the problem will probably be in some part of the address decoder. Make a check of the address decoder periphery circuits.

First check A14, A15 and RAS* signals to see if coming in properly. Unless these inputs are being made properly, and unless the output from Z64 pin 3 becomes "0" (but not staying at "0"), Z61 will not operate. Unless Z61 functions, no matter how properly the input of A10~A13 is made, nothing will happen.

Next, check A10 ~ A13. Check if proper output of 1Y0 ~ 1Y3 corresponding to A12 and A13 signals are being made. Also check that 1Y3 becomes "0" when A12 and A13 are both "1" and that this will cause output of 2Y0 ~ 2Y3 corresponding to A10 and A11 input signals.

If the above are functioning properly yet the decoder circuit still fails to operate, check Z60 and Z40, the gates for the Z61 output and also RD* signal.

CPU is constantly selecting the addresses and performing the data read/write. Especially it occurs usually that the keyboard is selected and read-in as memory. If some kind of false input is made at this time, CPU will think that the input is from the Keyboard and operate in unusual erratic manner.

(7) Keyboard

Since mechanical parts comprise most of tthe keyboard, first we'll explain repair of mechanical parts.

If the key spring is weakened or if there is a molded burr at the key cap, the key fails to return after pressed. In such a case, replace only the key switch or remove the burr.

The key switch contact can also be broken when keyboard input cannot be made. Replace the key switch.

Removing the key switch:

(1) Disassemble the main body and the entire keyboard unit.
(2) Remove the key top.
(3) Unsolder the key switch lead from the keyboard PCB, so that the lead is completely free from the board.
(4) Check the lead position. When the keyboard is faced up (the ten-key positioned at right side), the lead will be at right side.
(5) Use a long nose pliers and pull out the key switch from the key panel.
(6) Position the new key switch correctly and insert into the key panel till the switch sits properly. If this owrk is done with printed board laid on hard surface, care should be taken as the lead tip will not protrude up to printed board outer surface.
(7) Check the key switch is positioned correctly. Turn the PCB upside down and solder the lead.
(8) After soldering, insert the key top, and check for proper operation.

Short circuit in the keyboard matrix is the most frequent electrical trouble. If a character appears directly after >, there's a short circuit with the key for the character and PCB.

In case a different character appears when the key is pressed, press the keys on the same line or column on the keyboard matrix. If a character in a different line (or column) than the keys pressed is displayed, the lines (columns) of pressed key and displayed character are shorted.

In case the keyboard fails to operate at all, check for the damaged connection cable or faulty contact. It also could be that KYBD* signal is not coming from address decoder.

(8) Synchronizing signal generating circuit

If trouble develops in the synchronizing signal generating circuit, display indications will become unstable. If the vertical or the horizontal synchronizing signal fails to come out, trace the signal in reverse direction and check for defective points such as counter, select circuit, flip-flop, and others.

The system's main oscillator is used for the input to the synchronizing signal generating circuit, so if there is problem in the main oscillator, this could become the cause for the erratic or unstable display.

The synchronizing signal generating circuit output is utilized for video signal composition. So, the trouble in this circuit causes improper display. If the signal generated for horizontal or vertical display is faulty, check the synchronizing signal generating circuit. The first place to be checked is Z7 pin 11. The output here should be 50 Hz or 60 Hz. (The TRS-80 is available in both 60 Hz and 50 Hz models. In this chapter, the 50 Hz model figures are enclosed by parenthesis like "60 Hz (50 Hz)".)

If 60 (50) Hz, all counter circuits is operating correctly. If not 60 (50) Hz, trace the various counter outputs and check if there is a difference in the frequency.

In Fig. 5-5, the output frequencies of the various counters are indicated. Only the standard values are shown in this table. There could be slight variance from the actually measured values.

The frequency dividing ratio column indicates the division of the original frequency. For example, if the Z50 pin 8 frequency is 10.6445 MHz, the L1 value will become 7920 Hz (10.6445 MHz ÷ 1344).

Signal name	Signal output	Signal frequency 60 Hz	Signal frequency 50 Hz	Frequency dividing rate 60 Hz/50 Hz	Remark
VDRV	Z 7-11 pin	60.0 Hz	50.0 Hz	177408/212890	Vertical synchronizing signal
R8	Z 7- 8 pin	60.0 Hz	100.0 Hz	177408/106445	Character line
R4	Z 7- 9 pin	180.0 Hz	150.0 Hz	59136/70963.3	Character line
R2	Z 7-12 pin	360.0 Hz	350.0 Hz	29568/30412.9	Character line
R1	Z34-12 pin	660.0 Hz	650.0 Hz	16128/16376.2	Character line
L8	Z35-11 pin	1.320 kHz	1.320 (1.218) kHz	8064 (8736)	Each character line
L4	Z35- 8 pin	2.640 kHz	2.640 (2.437) kHz	4032 (4368)	Each character line
L2	Z35- 9 pin	3.960 kHz	3.960 (3.655) kHz	2688 (2912)	Each character line
L1	Z35-12 pin	7.920 kHz	7.920 (8.529) kHz	1344 (1248)	Each character line
HDRV	Z28-11 pin	15.84 kHz	15.84 kHz	672	Horizontal synchronizing signal
C32	Z28- 8 pin	31.68 kHz	31.68 kHz	336	Character line signal
C16	Z28- 9 pin	63.36 kHz	63.36 kHz	168	Character line signal
C8	Z28-12 pin	110.9 kHz	110.9 kHz	96	Character line signal
C4	Z34- 8 pin	221.8 kHz	221.8 kHz	48	Character line signal
C2	Z34- 9 pin	443.5 kHz	443.5 kHz	24	Character line signal
C1	Z27- 7 pin	887.0 kHz	887.0 kHz	12	Note 1
Chain	Z27- 9 pin	887.0 kHz	887.0 kHz	12	Input

Note 1: In the case of 64 character display.
Note 2: Values in parentheses indicate that the one in 5 cycles out of 26 cycles of L8 included in 1 cycle of VDRV in case of 50 Hz specification.

Figure 5-5. FREQUENCY OF SYNCHRONIZING SIGNAL GENERATING CIRCUIT

When the frequency differs considerably, an approximate correct frequency signal can be found by tracing up this chart. However, the conclusion that this place is faulty should not be given out hastily.
For example, trouble was suspected to the place where the HDRV signal come out, but the C32 turned out to be good. In such case, Z28 counter may be defective, but trouble could also be in IC's like Z5 and Z62. This is due to the effects of periphery circuits.
Before replacing the IC's, cut the printed wiring on printed board with knife tip. Cut the Z28 pin 11 and recheck. If correct value is still not indicated, replace Z28.
If operation was corrected after cutting pin 11, repair the cut part carefully by soldering. Next cut the Z5 pin 11. Recheck Z28 pin 11, and if signal is coming out, replace Z5.
Determine what portion (part) is defective by cutting and resoldering the printed board circuits in the above manner.

(9) Video RAM
In case the video RAM fails to work properly, faulty multiplexer could be possible. Check the Z8, Z29 and Z36 common input pin 1. to see if siganl is coming in. Check pin 15 to see if grounded and pin 16 to see if power is supplied. If all are satisfactory, and if the address from CPU and signal from synchronizing signal generating circuit are not coming out properly from output pin, try to replace the defective multiplexer.
Check all address lines to the video RAM. In the case of 64 character pattern display, pulse signals are sent in so there is no floating or fixed signal. If there are such signals, the cause could be address line short, pattern defect, or multiplexer defect.
Check the video RAM pin 10 signal. This terminal is normally at Logic 1, but on pressing the key, Logic 0 signal appears. This is from the CPU to write the video signals.
If the multiplexer is free from trouble, video RAM pin 10 is normal, and address signal is also normal, try to replace the video RAM.
Remove the ROM and turn on the power. The display will be fully covered with @9 at 64-character mode and with @ or 9 at 32-character mode.
If only a part of the above appears, try adjusting the display. If in horizontal direction, @9 appears in only a few lines, check the line addresses V6-V9. If in vertical direction, @9 fails to appear, check the column addresses V0-V5.
If the display is flickering (when @9 is displayed), CPU is continually interfering in video RAM address circuit. If at this time, the video RAM address is observed, the address by synchronizing signal and the address signals from CPU are alternately coming out, this is a normal condition.
Unless there is such flickering, it would mean that the CPU signals are not being transmitted to the multiplexer.

(10) Video formation circuit

When the video formation circuit becomes faulty, some of the dots in characters become missing, or may go completely blank.

The video formation circuit is in cascade connection, making it relatively easy to detect source of trouble.

For example, if characters appear but graphics fail to appear, it will only be required to check the periphery of shift register Z58 and graphic generator Z11.

When graphics appear but characters do not, check the periphery of character generators Z37 and Z38 (Z38 for levels I and II, and Z37 with character generator inserted or level II Kana), and shift register Z57. When characters and graphics fail to appear, check will have to made up to Z54, Z55, Z56, Q1 and Q2.

The worst trouble is when nothing appears on the display. Where would the best place be to start?

First of all, check the power supply. If the power supply voltage is not normal (too low), nothing may appear on the display. Next, check the main oscillator.

If this is normal, check the video signal at Q1 emitter. From this last output, check in reverse direction until the place is located where the signals are coming out.

Before going too deep with this reverse direction method, check the character generator to see if signals are coming out. If this is normal, the trouble would be between these two points.

Let us see what the TRS-80 is doing at this time. For example, if it is trying to produce characters, there will be pulse signals at Z55 pin 6, and moreover, if there are signals coming out from Z57, then check Z54.

If Z54 pin 12 is at Logic 1, there will be no output from pin 13. If Z55 pins 6 and 8 are both at Logic 1, it can be considered that Z56 is not operating. It could also be considered that Z53 is faulty.

If nothing appears on the display, pull out ROM and try to have @ 9 appear over the entire display.

The following are some of the procedures to be used as reference when looking for trouble.

(i) Display characters and patterns are dim.
Z3 could be bad. If Z3 tends to get hot, replace it. When hot, the transistor saturation voltage rises, making Z3 unable to drive the Q1 transistor and as a result, the picture will become dim.

(ii) When character dots are missing.
When some part of all characters have missing dot rows, check the input to character generators RS1, RS2 and RS3.
If correct input is being made, replace the character generators. If the dots are missing in the vertical columns, check the input to Z57. If proper input is supplied, replace Z57.

(iii) Character display dots unstable.
When Z57 temperature rises, Z57 may miss data when loading, resulting character display dots to become unstable.
If Z57 heats up abnormally, or the above symptoms still appear when cooled, replace Z57.

(iv) Graphic parts missing.
Check the input to Z39. If the input is proper, check the output.
If the missing occurs in vertical direction in either the left or right side pattern, the problem would be in Z39 periphery.
If vertical lines appear in the graphic, Z58 is defective.

(v) Graphic unstable
The cause would probably be the same as in (iii) above. Depending on the condition, replace Z58.

(vi) No inter-character line blanking.
This relates to L8 signal. Check the synchronizing signal generating circuit, and in addition, the Z56 latch.

(vii) Display interference develops.
This is not a video formation circuit problem. Check the +5 V circuit signal. If oscillating, check C11 or C16 (+12 V side) to see if it is operating properly.

(viii) Spelling errors
If mis-spelled words appear, check for faulty data from video RAM, defective Z11, and if character generator address line from Z11 is shorted or is open.

(11) Synchronizing signal composition circuit

This circuit is mainly composed of AND, NAND and NOT gates. Check this circuit in case of inability to synchronize the display picture even when there is proper output of HDRV and VDRV signals.

This circuit determines the horizontal and vertical synchronizing pulse widths and timing, so this circuit should be checked if the display is too high, too low, or too far to the left or right.

In case the horizontal direction appears faulty, check the Z51 pins 13 and 12 and its output pin 11 to see that they are in proper relation. Also check the Z61 pins 1, 2 and 3 to see that they are corresponding properly with pin 5.

In case the vertical direction is bad, check the Z52 input-output relationship and the JP7 and JP8 to see if correctly inserted or shorted.

In case the above are in proper condition, check the Z32 input-output relationship and JP6, JP7, JP8 and JP10 to see if the signal is correctly inserted. If these are in proper condition, the problem would be in sysnchronizing signal generating circuit or the video formation circuit.

(12) Address Decoder

The address decoder is made up of gate circuits. Check the gate inputs and outputs to see that they are properly corresponding.

For example, even if the ROMA* and MEM* signals have been verified to be coming out, but it would be difficult to determine if the ROMA* signal is coming out accurately at the precise time. This could be checked by the following method.

(1) Check all inputs to address lines, and by logical analysis, confirm that ROMA* is being sent out.

(2) Designate the ROM address already known by CPU by preparing machine language program or by installing address switch.

When address decoder becomes defective, the operations of other parts could also become defective.

When power is turned on and READY or MEM SIZE? is indicated, there are cases when the keys fail to operate. At such a time, check the KYBD* signal.

If this signal is not sent out, the decoder concerned with KYBD* could be at fault. However, if READY or MEM SIZE? is displayed at this time, there should not be much problem.

In case power is turned on and the initial indication (READY at Level 1, MEM SIZE? at Level II) fails to appear, what should be done? The thing that could be thought of is that the RAM is not working. Check the RAM* signal.

If the Z64 pin 11 is not showing output, check Z64 pin 4 for input RAS* and pin 5 for A15 signal, and Z44 pins 12 and 13 for A14 signal. If these are all satisfactory, Z64 could be defective.

There is a method of removing the ROM for checking the several signals sent out from address decoder. If the CPU is in normal state, removing the ROM will allow ROMA*, ROMB*, VID*, RAM*, MEM* and most of the other decoder outputs to appear. This makes it possible to check the decoder state.

(13) Cassette recorder control

When using the cassette recorder, if it is in normal state, it will start off with a click and the motor will start turning, but there are cases when the motor fails to turn.

The cause for this could be the relay K1 being faulty. This relay is located at the back side of the cassette cable insertion connector J3.

Relay malfunction could be caused by defective contacting of relay points or by short or open circuit in relay coil.

Short circuit in relay coil will create the state of Z3 pin 5 being shorted to Vcc, with possibilities of damaging the Z3. If this happens, video display will become blank as the Z3 is also used on video circuit.

Thus, if the video display should suddenly become dim or go blank, the cause could be short in relay coil or in CR4.

If the K1 relay contacts should remain closed, try removing the K1 relay with fingers. This will open the contacts with no danger of the motor stopping.

The contacts could remain closed when the motor is operated through the application of CLOAD, but if this happens too frequently, replace relay K1.

(14) Cassette recorder input-output circuits.

If problems arise when data or program input is made from cassette, check the Z25 pin 9 signals.

Make the input with long program: at this time, observe pin 9. This pin is normally at H level, but changes to L level with signal entry. If two pulses are sent out successively with each bit time, it could be assumed that Z25 is functioning properly.

If there are problems in CR5 and CR6 or CR7 and CR8, Z25 pin 9 would normally be at L level but could change to H level when the signal arrives from the tape.

The reason for this is that CR5 or CR6 was shorted or CR7, CR8 or C41 was defective, they become unable to perform level detection.

For these operations, refer to the operational explanation in Chap. 3.

If the flip-flop input for Z31 set/reset is working properly, input a long program with CLOAD and check the Z31 pin 8. If the output is being made properly from pin 8, check the Z59 pin 1 input and pin 5 output.

While performing the CLOAD, reset the Z31 flip-flop with OUT*. If Z31 remains set, check the Z40 pin 6 signal, and then check the input to Z40 pins 4 and 5.

If INSIG* is not operating, check Z40 input pins 1 and 2. If both INSIG* and OUTSIG* signals are not coming out, check the input signal to Z41 in address A0~A7 decoder circuit. Unless the address A0~A7 becomes FF, 0 will not be sent out from Z41 pin 8.

If all signals are correct and Z59 is normal, check the RAM, CPU and ROM in this order to determine the location of the problem. One of the methods is to compare with the normally operating TRS-80 INSIG* and OUTSIG* changes when CLOADing.

RAM could sometimes be determined whether faulty when performing CLOAD. For example, there are cases when the program can be entered in normally up to a certain point but from then on, nonsense data starts to enter in.

In such a case, replace the RAMs one by one to enable locating the defective RAM.

When performing CSAVE, it seems that poor recording is usually due to CPU rather than ROM.

Check the CPU. If there seems to be no problems in CPU, check the IN* and OUT* signals, and after this, check the ROM.

If the problem appears to be in CSAVE, just assume that the cause is in the software (ROM/RAM) and latch (Z4).

If the CLOAD is found to be operating correctly, without setting the tape in the recorder, try CSAVE of the program and check the J3 pin 5 output waveform. If waveform fails to appear here, check the R2, R3 and R4 resistors and also Z4 pin 9 OUTSIG*.

When CSAVE is performed, D0 and D1 values are latched by Z4 and used, so check these two data lines. Check Z4 pin 1 to see if at Logic 1.
Failure in 32-character display operation could also be caused by trouble in this Z4 latch. This is because the output MODSEL from Z4 pin 6 latches the D3 values at OUTSIG* clock pulses.
If CSAVE and CLOAD are operating properly, faulty latching of Z4 pin 6 output or ground or short of Z4 pin 6 could be the cause.
Z4 latch can be cleared by grounding Z4 pin 1. When this latch is cleared, the 32-character display will change into 64-character display. If on removing the ground from pin 1, the display returns to 32-character mode, the probable causes would be OUTSIG* signal entering into pulse signal,is removed or line breakage in printed circuit board causing noise.

(15) Power supply

Power supply problems arise from defective soldering, component shorts, solder shorts, and open circuit in power transfromer.
Power supply will not be damaged by output terminal short because of current protective devices. Thus, solder shorts and other troubles can occur outside the power supply, but the voltage will not fail to appear.
When voltages from +12 V and +5 V power supplies fail to appear, measure the voltage at both R30 terminals. If this voltage is 0.6 V, the +12 V is not appearing since its power supply is shunted off through feed back circuit.
Unless +12 V is impressed, +5 V Voltage will not appear. This is because the +5 V stabilizer Z1 IC uses the output from the +12 V. In the above case, check for short in the +12 V supply.
If the −5 V power is not present, measure the voltages at both ends of R12 resistor. If a total voltage (−11 V) is impressed on both ends, there is a short somewhere.
The +12 V and −5 V are used only as RAM power supply so if one of them appears to be shorted, the short could be inside the RAM. A RAM with an internal short will become much hotter than the other RAMs so that it can immediately be detected by touching with finger.

CAUTION

When checking the RAM with finger, use sufficient care because a shorted RAM can heat up very high to cause burns.

If +12 V fails to appear, touch the heat sink in the Q6 transistor with finger. If very hot, RAM has broken down and is shorted.
In case +12 voltage does not appear and if it is not known whether the power supply or RAM is at fault, open the power switch, trace the +12 V pattern and cut the pattern at the place just before entering into the RAM.
Turn on the power, and if +12 V appears, the RAM could be faulty. If voltage fails to appear, check the power supply circuit.
RAM.
Locating short in +5 V power supply is very difficult. Since this +5 V is supplied to numerous places, shorts are more likely to occur.
First of all, carefully make visual check for solder short and the like. If unable to locate, cut the wiring on printed circuit board. In this case, the short can be located faster by using the two-division method.
First cut the +5 V line near the middle. It there is a short, it could be in the rear one-half from the cut point, or it could be in the front one-half from the cut point.
On the section believed to be shorted, cut the line in half and make the check. On the portions found to be free from shorts, connect by resoldering. When soldering, use care not to apply the hot soldering iron too long as there will be danger of peeling off the printed circuit.
Use the above method and make repeated check for shorts.
If the +12 V power supply appears to be faulty, first check the Q6 heat sink. There have been cases of the screw loosening and causing base or emitter to short on the heat sink. At times, transistor legs have loosened off from the printed board. If heat sink screw is loose, retighten using care not allow base or emitter to short on the heat sink.
AC adapter troubles are usually defective terminal connections. Check the fuse and other wiring. Also check the DIN connector if the wiring is loose.
If the fuse blows out easily, check for short in diode inside the rectifier CR1.

Fig. 5-6 indicates the values of the Z1 and Z2 pins when functioning normally. Adjust +12 V to 12.00 V and +5 V to 5.00 V.

Pin No.	Z1 Voltage	Z2 Voltage
1	0.00	0.00
2	5.33	10.55
3	4.99	12.00
4	4.99	7.28
5	4.99	7.28
6	7.23	7.28
7	0.00	0.00
8	0.00	0.00
9	0.60	5.61
10	5.96	12.31
11	12.00	25.80
12	12.00	26.70
13	7.10	13.54
14	0.00	0.00

Note: These voltages are those measured against C10 capacitor GND side with digital voltmeter (DC range).

Figure 5-6. VOLTAGES OF Z1 AND Z2 PINS

(16) Horizontal and Vertical Adjustments

In TRS-80, all video sychronizing signals are made up in the digital circuit so picture position should not change each time. However, if the picture position should seem to have shifted due to some logic defect or the video is out of adjustment, enter the following program and confirm. This program can be used on both Level I and Level II models.

```
10 CLS
20 FOR X = 0 TO 127
30 SET (X, 0): SET (X, 47)
40 NEXT X
50 FOR Y = 0 TO 47
60 SET (0,Y): SET (127, Y)
70 NEXT Y
80 FOR X = 62 TO 65
90 SET (X, 23): SET (X, 24)
100 NEXT X
110 GO TO 110
```

5-4. Intermittent Troubles

The TRS-80 could develop trouble and just when steps have been taken to repair it, the TRS-80 returns to normal operation. Then it is operated to get some work done, a lot of meaningless display starts coming out. At such a time, some people recommend striking it several times, but such practice should be avoided.

In this case, load a test program from a cassette or floppy disc, and try checking the memory. Also at this time, make the memory check continously and as long as possible. Long time memory check could result in indication defective memory. If nothing happens, try to replace all of the RAMs.

If test program fails to get results, try making up a program that will surface the trouble. To trace down a trouble that occurs only once in a long while, try making a program which contains many of the would-be errors.

For example, if the display becomes erratic in FOR-NEXT loop, then use a lot of FOR-NEXT statements and run a program to see if it will form erratic display.

The trouble could be due to improper contact caused by faulty soldering. At such case, lightly tapping the printed board with eraser end of pencil could sometimes enable locating the defective contact.

A solder ball could be rolling on the printed board. If lucky, it could be rolled out by lightly tapping the board. It also may lodge tightly somewhere.

In any case, if the solder ball is found, it can be assumed that this is the cause of trouble; remove it.

Carefully check the soldering at all parts especially at ICs, resistors, and capacitors.

For intermittent troubles, check the through holes on the PCB that solder completely fills the holes without breakage.

If through hole appears doubtful, insert a fine wire and solder.

5-5. Troubleshooting Hints

One of the difficult points in troubleshooting is the presence of machine language program in ROM. Since this program controls the CPU, fairly bothersome trouble must be overcome to understand all of the operations. There are also times what the CPU is doing is unknown.

At keyboard explanation, the keyboard operation was only briefly taken up. No detailed explanation was given.

If the software should conceal a defect somewhere, what methods should be taken in troubleshooting? In regard to what parts comprise the keyboard software, and how they operate, would there be any necessity for expending large efforts in making detailed analysis on the various operations of the program? As long as there is no time to be wasted, it is not recommended to make a list of all softwares and decide what part of each software is defective.

Thus, in this section, it is assumed that there is no fault in the software, and a check is made on the kinds of malfunction in the hardware.

This kind of policy will determine whether the trouble has actually developed at that part. If it has been accurately determined that the trouble is not in the hardware, it will become evident that the problem will be in the ROM (the software).

(1) Steady output gate circuit.

When a gate is checked with an oscilloscope, the pulse signals are so numerous that it will be difficult to determine whether it is operating properly.

An effective means for troubleshooting are:

Ground the gate input side pin. Under some condition, this will not harm the TTL. For example, if output does not appear at OR or NOR gate, try grounding one of the input pins.

If normal output appears at this condition, you can see that at least the unshorted side gate input is operating normally. Try shorting the other input pin, and if the output can be seen, this gate is operating properly, so move to the next step.

In checking the NAND or AND gate output, to ground the input pin as above would not help (except when AND gate output is constantly at Logic 1, or when NAND gate output is constantly at Logic 0.)

Never connect the input pin to 5 V power supply. This could damage the output side of other TTL connected to the input. Try as much as possible to find places where the check can be made by grounding the input pin.

For example, on video signal generating circuit, Z50 pin 10 is the inverter output to Z55 pulse generating circuit input. To make the Z55 input pins 4 and 12 together to Logic 1, Z50 pin 10 is grounded.

If the signal cannot sent out from the output side by grounding the input as above, the chances would be

(1) Gate is damaged

(2) Output side is shorted to +5 V Vcc or to ground.

To check either of the above, cut the printed board lines to check the output from output pin only. If this causes the proper output to come out, there is a short some place in the output side wiring. For example it could be shorted with an IC for some other input.

Check the printed board lines for shorts. If the IC is defective, replace it. Reconnect the cut pattern with jumper wire to restore former state.

The IC damage may be cause by a short circuit in +5 V line. If it seems so, check by measuring the gate output voltage. If there is a short in the line to Vcc, +5 V will be indicated. H level at TTL is normally only around 3.7 V. (The output in case of CMOS is only a few millivolts lower than the power supply voltage.) If it is found that there is a short with +5 V, check the lines on the printed circuit board.

For the short to the GND side, the check can be made by the above method. In this case, use an oscilloscope. Place the probes on the line suspected to be shorted and open the power switch. If the value stays constant, it can be assumed that the line is shorted.

When the power switch is opened and the voltage rises once and then drops, that line could be shorted with the output pin of another TTL.

(2) Types of shorts

In the causes for shorts, the following five are most common.

(1) Short caused by solder splash.

(2) Short caused by solder ball or metallic particle entry from outside.

(3) Short caused by solder hair.

(4) Short caused by insufficient etched part in printed pattern.

(5) Short cused by defective component.

Short arising from splashed solder is very common. This will result in short between pins. This type of short is easy to detect.

In the short arising from solder ball, the balls are formed by the automatic soldering machine even after the printed boards are washed, the small solder balls can sometimes remain on the board.

The solder hair can cause short between IC pins and between patterns and it is extremely difficult to detect. When cutting the pattern with a knife to detect trouble, use care not to make any metal splinters.
Insufficient etching causes pattern short. Short can also develop between patterns in case the printed board is damaged.
If too much time is taken in soldering the printed board line, the line will heat up and peel off from the printed board. This peeled off line can result in forming a short, or cause stoppage due to cut pattern.
Defective IC or diode can sometimes cause short between Vcc and GND.

(3) Logic shorts

If TTL gate outputs become shorted together, strange actions may occur. For example, some functions may work normally but may work abnormally at times.
In case of multiple shorted gate outputs, tri-state element type of signal may appear. In the signal level of tri-state element, there seems to be another logical level between the logic "1" and logic "0."
Normally, the TTL output never shows any operation like the tri-state element, so if a waveform similar to that of tristate element should appear, make a careful check of the pattern to see where the printed patterns have shorted together.
In most cases, the short will be on the printed board, but in very rare cases, the outputs from a single IC may be shorted together within the IC package. In such a case, replace the IC.
In the synchronous generator circuit, 74LS93 is used as the counter. When the counter output side waveform is observed with oscilloscope, it could be found to contain many levels.
In these levels, the counter clock pulse intervals will be constant. In case of such counter, there may be many levels, but unless they fall below the level (2.4 V) at which the TTL input operates at Logic 1, there will be no abnormal operation.
The counter output variation is around 0.5 V, and even when the output is at its lowest, it still will be above 3.0 V. Such properties are peculiar to the counter output so that unless they are known, it will be thought occasionally that the counter output is peculiar.

(4) Address and data bus shorts.

Address and data busses run parallel on the printed board, so shorts between these busses frequently occur.
In addition, these busses go to all aprts of the system and even go outside via connectors.
Normally shorts would occur on data bus more frequently than address bus, because the data bus is a tri-state element and data can be transmitted in both directions.
In the address bus output buffer, tri-state element is also used, but in ordinary operation, tri-state is not functioning. Check in a same way as ordinary TTL. However, when TEST* input is grounded, the address bus goes into floating state.
In the case of address line, check the address line waveforms successively with oscilloscope, and see if at any place, two lines are operating in same manner, and moreover, in tri-state element manner.
If such signal is observed, there is a short between the address busses. Make a through check on printed board for short between the two lines. In such case, there are often troubles such as solder hair stuck between IC pins, or pattern bridge formed between pattern and IC pins, or by etching error.
If the short cannot be located, cut the line to check, (make sure to repair the cuts).
In checking data bus shorts between lines, using the same method as for the address bus of looking for same signal on two lines will not do, because the data bus is in tri-state operation same kind of signals will frequently be on the data bus.
When checking data bus, even if TEST* is grounded, data bus will not go in floating state like address bus. However, by cutting off the pattern from Z23 pin 9 to GND, and sending the Z46 pin 10 output into Z23 pin 19 as input, dropping the TEST* to 0 will cause the data bus to cut off from the CPU and go into floating state.
Check the bus lines, and if at Logic 0, the buffer IC (Z23) is defective. Try grounding the bus lines one by one, and if the other bus lines are showing ground potential, without being grounded, there will be a short between these bus lines.

(5) Bent pin

In TRS-80, some of the ICs are provided with sockets. Check these socketed ICs to see if any of their pins are bent.
If bent, defect contact could develop between the socket and IC pin. Care should be taken on these socketed ICs as they are CPU and ROM.

(6) Jumper wire connection

In TRS-80, a large number of jumper wires are used. These jumper wires should be properly checked as correct operation will not be performed if incorrectly inserted. Jumper wire connections are as shown in following tables.

If CRT fails to synchronize or remains blank, refer to Table (2).

If computer fails to operate or characters do not appear on CRT display, refer to Table (1) or (3).

Make sure which version you are going to use before make comparisons with the connection lists.

Connection Table 1.

	JP1	JP2	JP3	JP4	JP5
Level I	X	X	X	C~2	C~2
Level II	O	O	X	C~2	C~2
Level II Kana	O	O	O	C~1	C~1
Level II Kana Small letters	O	O	O	C~1	C~2

Connection Table 2.

	JP6	JP7	JP8	JP10
CRT Frequency 50 Hz	C~2	C~2	C~2	C~2
CRT Frequency 60 Hz	C~1	C~1	C~1	C~1

Connection Table 3

	JP9
Level II Kana	X
Level I Level II	O

Note 1: X indicates without jumper wire.
O indicates with jumper wire connected.

Note 2: C~1 indicates C and 1 connected with jumper wire.
C~2 indicates C and 2 connected with jumper wire.

Figure 5-7. JUMPER WIRE CONNECTION TABLES

6. THE OUTSIDE WORLD

After you start using the computer, you may become ambitious to use it for various purposes. This section will discribe a method for connecting something to your computer and try doing some kind of a job.

By utilizing software only, many things can be done with the TRS-80. However, if that becomes insufficient, you may want to connect the another hardware and seek further applications for the computer.

For this purpose, a detailed knowledge of the software will be repquired first of all.

For Level 1 Basic, a certain amout of knowledge on the methods of making up a program in machine language will be required.

In Level II Basic, relatively simple commands like "POKE" and "PEEK" or "OUT" and "INP" can be used. By using Basic, control can be exercised on interface that can be connected with relative ease to the outside.

If utilizing the machine language seems to be too much of a job, use "Editor/Assembler", which makes programming in machine language relatively easy.

In any case, if anything is connected to the outside, software will always be required for controlling the outside circuit.

Even if expansion interface is attached to TRS-80, except for disc and printer device, hardware for control of special outside devices is not available.

For example, it would be very convenient if a system could be made so that at certain pre-set time the air-conditioner will be switched on, the pot will start boiling the water. Then when breakfast preparations are made, the TV or the radio will be turned on.

To work out, the interface have to be designed for such purpose.

To design the hardware, you have to decide which control you have to adopt after broadly dividing the TRS-80 in two parts. In connecting the control device, there are two methods:

(1) Connect as part of the memory.

(2) Connect as an input device.

When utilized as a part of the memory, consider what part of the memory should be allocated as the address.

In order to use this as a part of the memory to control the outside interface, 16 address lines and 8 data lines are used.

Then in order to control this as an interface output unit, WR* signal is used. When the outside interface condition is to be checked by the CPU, RD* signal is used.

When the program is to be made up in machine language or by assembler, LD (Load) command is used for controlling the interface connected to outside, "POKE" and "PEEK" are used at Level II Basic.

For example, take the case of interface having the objective of supplying standard AC power supply. Controlling this AC voltage power supply will differ with the relav contact permissible current, but to allow use for any purpose, hex address indication 8FFF is allotted, and interface made to have the power "ON" at data 02. With the Assembler, this becomes

LD (8FFF), 02 H, POWER ON

This assembler is converted to machine language and through the performance of this program, 8FFF memory is designated and the power goes "ON" when the data becomes 02.

At Level II Basic, POKE execution statement is utilized, and written

POKE - 28673,2

This - 28673 is the hex 8FFF expressed as decimal number.

Instead of memory allocation, there is a method of controlling outside interface circuits by utilizing input and output ports.

In this case, CPU can control a maximum of 255 input-output devices. For example, assume that to control the power supply circuit, the circuit address is indicated FE in hex number, and data 02 and designed at these values. The assembler program made at this time will become

OUT 0FE, 02 H, POWER ON

And when written in Level II Basic, this becomes

OUT 2542

Both execute exactly the same thing. 8 address lines and 8 data lines are used at input-output ports use. To perform at the input and output ports, OUT* and IN* signals are used.

It is free to use the above memory allotment or the input and output ports to perform control of the outside interface, but when many RAMs as possible are installed in the TRS-80 (maximum 48 K bytes), memory allotment space is virtually eliminated so that hex number 3000 - 36FF and 3900 - 3BFF range cannot be utilized. (3700 - 37FF range is used in expansion interface. Since Kana version uses 3000 - 33FF, utilization possible is 3400 - 36FF).

There are 256 kinds of input and output ports, 0 - 255 (00 - FF). For cassette tape recorder control, hex FF is utilized. Since E8 - EB are for RS232 purpose, addresses other than these must be used for control.

In memory allotment, 16 address lines will be required but when input and output ports are utilized, 8 lines will be sufficient to make the hardware design much more easier.

(1) Example of outside interface for power supply circuit control by memory allotment

Fig. 6-1 shows an example of an interface for power supply circuit control by memory allotment mode. This is just one example and others can be designed by using different methods.

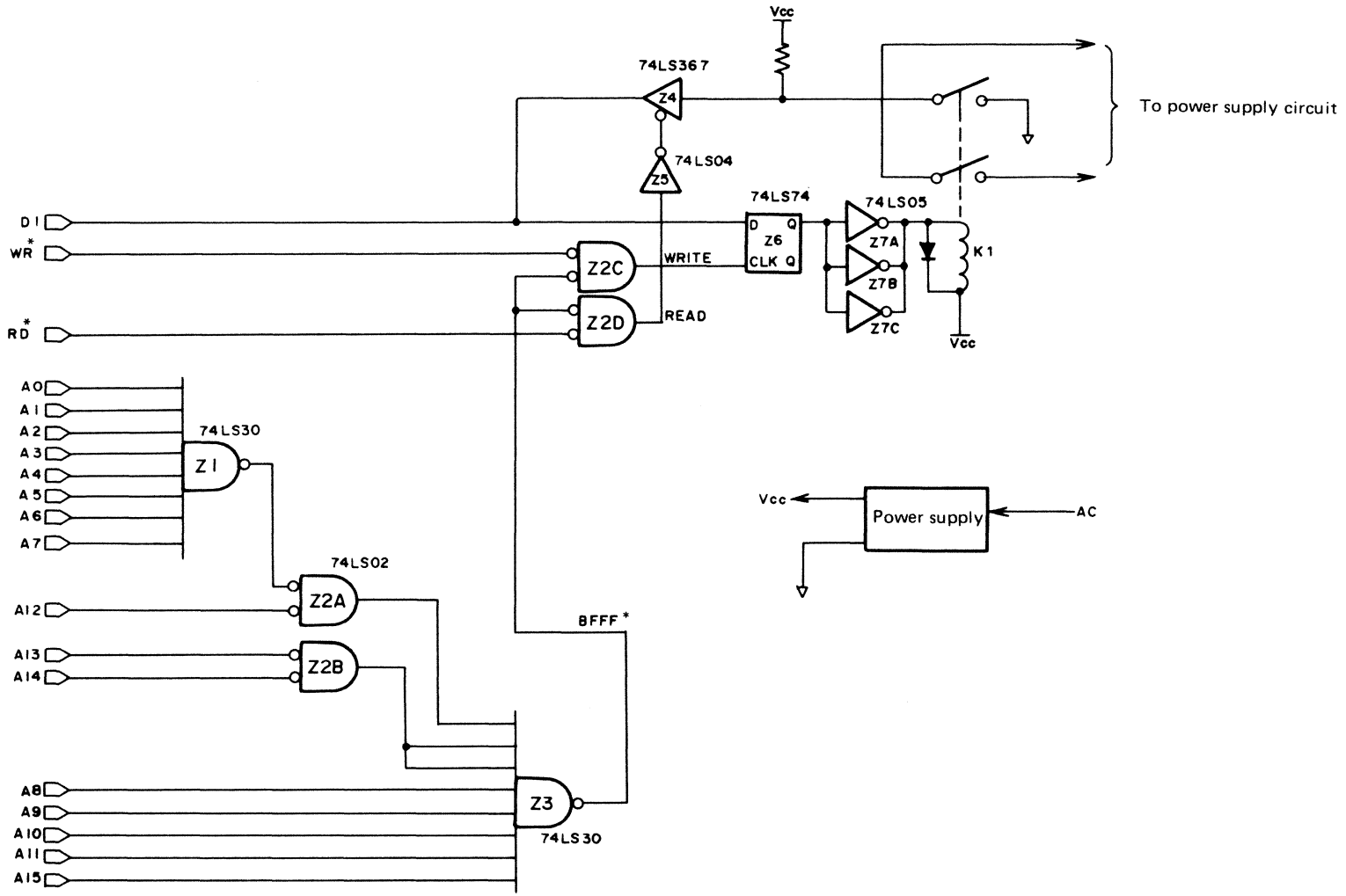


Figure 6-1. EXAMPLE OF POWER SUPPLY CIRCUIT CONTROL BY MEMORY ALLOTMENT

Conditions regarding software are:

(1) Relay control necessary for controlling power supply circuit.
(2) Allot hex 8FFF for memory address.
(3) Check relay if "ON" or "OFF."

Circuits for decoding memory addresses are Z1, Z2 and Z3. When 8FFF address is given, 8FFF* signal becomes Logic 0, to satisfy the input conditions for Z2 C and D input gates.
POKE statement will use the decimal address - 28673 conforming to Hex 8FFF and become

POKE - 28673,2

When this is executed, WR* signal becomes 0, C output of Z2, that is WRITE signal is given out, and becomes Z6 clock signal. Hex 02 data causes D1 signal to become Logic 1, and flip-flop Z6 to set.
When Z6 output becomes H level, Z7A - Z7C relay drivers work and allow current to flow to K1 relay, causing power supply circuit contacts to close.
The K1 relay opens when at

POKE - 28673,0

In order to check the status of the power supply circuit control relay, PEEK statement is utilized.

If the relay is closed, current will be flowing into K1 relay. When the power supply relay contacts close, the contacts on the other relay will also close at same time, resulting in grounding the Z4 input. As a result, the Z4 input side will become 0 V.
If PEEK statement causes

A = PEEK (−28673)

8FFF* signal will become Logic 0, and RD* signal will become Logic 0 and fixed output will be seen at Z4 3 element output end due to input value.
As a result, the relay will actuate and at ON state, D1 output becomes 0. When relay is off, that is, when power circuit is cut off, it becomes 1.
This output connects to D1 so that the read out data becomes

D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	X	X	X	0	X	relay "ON"
X	X	X	X	X	X	1	X	relay "OFF"

X indicates 0 or 1 is unknown.

Thus, in order to know the relay status, the following Basic program will be required.

800 B = 2
900 IF (A AND B) = 0 THEN GO TO 1980

At (A AND B) = 0, this indicates that relay actuated, and at this time, the line number 1980 in program is being executed.
The following are the precautions in making up the interface.

(1) Provide proper decoder on address.
(2) After perfoming WRITE function, perform READ function to check for correct operation.
(3) Latch data from data line (may not always be necessary).
(4) Provide separate power supply.
(5) Do not allow more than one LS type TTL load at the output of the computer.

The above (4) and (5) are very important. Failure to observe them will result in improper operation.

(2) Example of outside interface for power supply circuit control by input-output ports

Fig. 5-2 shows an example of an interface for power supply control by means of input and output ports. The circuit at the right side of Z2 is identical with that in Fig. 6-1. The only difference with Fig. 6-1 is that OUT* is used instead of WR* and IN* instead of RD*.
In designing an outside interface with input-output ports, 8 address lines are used. Z1 and Z4 addresses are Hex FE that have been decoded. This FE corresponds to decimal number 254.
In the case of writing with Level II Basic, POKE is written

OUT 254,2

and PEEK is written

A = INP (254)

By means of the above, the same operation can be performed as with POKE and PEEK.
Through OUT 254,2 statement, FE* output of Z1 becomes Logic 0, Z2A or Z2B goes into operating state. When at OUT, the OUT* signal becomes Logic 0 and signals are sent out from WRITE.
At INP, IN* signal becomes Logic 0 and signals are sent out from READ. Z4 status element 3 input conditions are then sent out over D1 data bus.
As related above, the difference between performing memory allotment of performing the control with input and output ports lies in the use of the address busses and the use of signals WD*, WR*, OUT* and IN*. However, in the operation itself, there is no substantial difference.

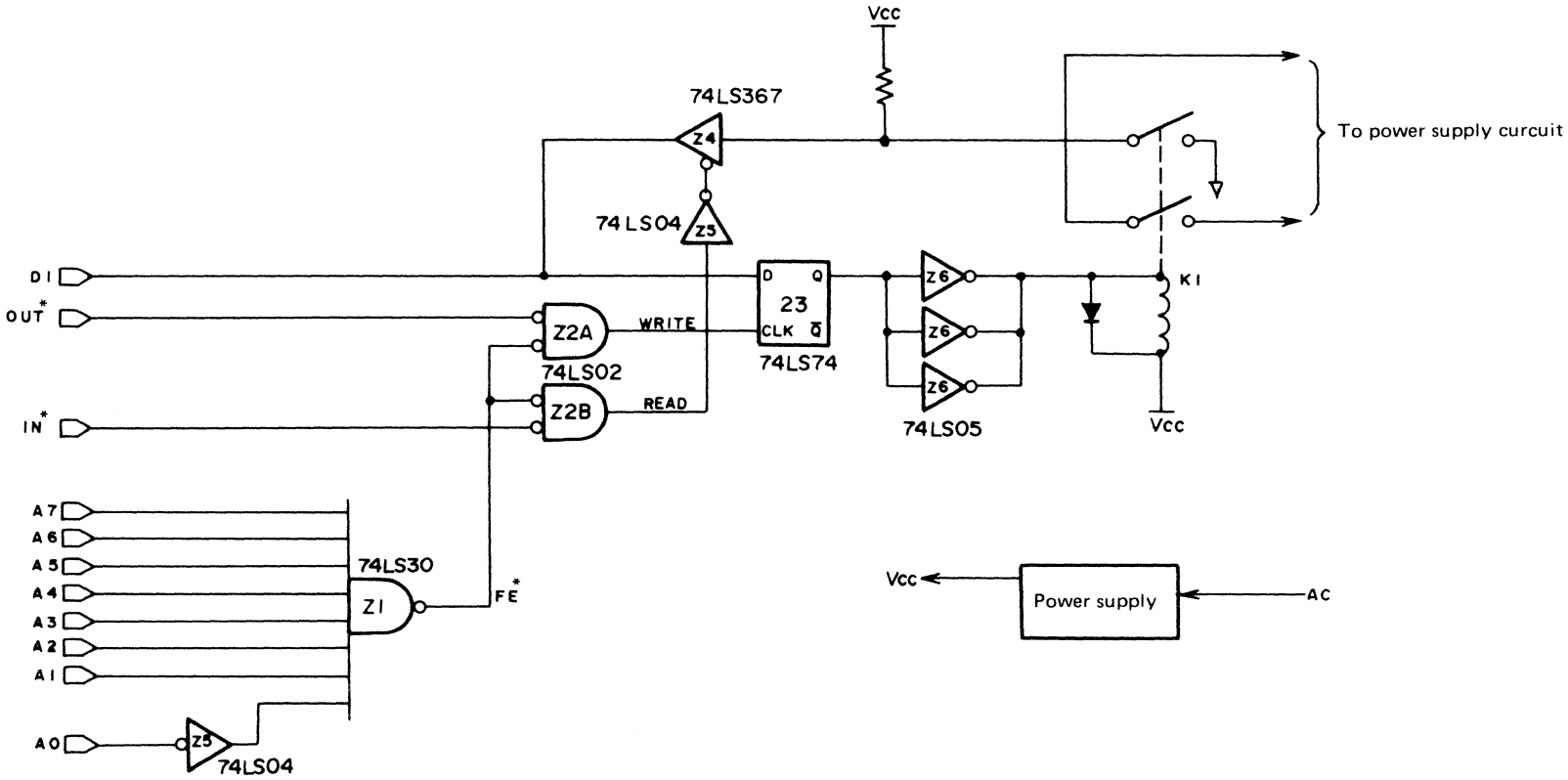
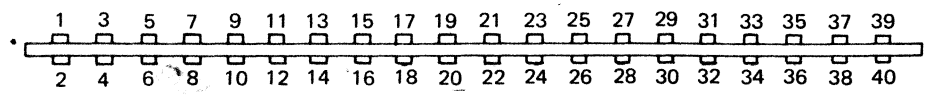


Figure 6-2. EXAMPLE OF POWER SUPPLY CIRCUIT CONTROL BY INPUT-OUTPUT PORTS

Pin Connections for Expansion Interface Connection

Pin No.	Signal Name	Description
1	RAS*	Row address strobe signals for dynamic RAMs
2	SYSRES*	System reset output
3	CAS*	Column address strobe signal for dynamic RAMs
4	A10	Address output
5	A12	Address output
6	A13	Address output
7	A15	Address output
8	GND	Signal ground
9	A11	Address output
10	A14	Address output
11	A8	Address output
12	OUT*	Strobe output for output devices
13	WR*	Memory write strobe output
14	INTAK*	Interrupt acknowledge signal output
15	RD*	Memory read strobe output
16	MUX	Dynamic RAM address change signal
17	A9	Address output
18	D4	Data input-output
19	IN*	Strobe signal for input devices
20	D7	Data input-output
21	INT*	Interrupt input (Maskable)
22	D1	Data input-output
23	TEST*	Input terminal for test
24	D6	Data input-output
25	A0	Address output
26	D3	Data input-output
27	A1	Address output
28	D5	Data input-output
29	GND	Signal ground
30	D0	Data input-output
31	A4	Address output
32	D2	Data input-output
33	WAIT*	WAIT input
34	A3	Address output
35	A5	Address output
36	A7	Address output
37	GND	Signal ground
38	A6	Address output
39	GND	Signal ground
40	A2	Address output

Note: *means negative logic (Active, low)



Mates with AMP P/N 88103-1 connector or its equivalent.
Note that pin numbering method differs from connector pin numbers.

Figure 6-3. EXPANSION INTERFACE CONNECTOR SIGNALS (viewed from rear of keyboard assembly)

7. TWO TYPES OF TRS-80

TRS-80 Microcomputer System Model 1 main body can be roughly classified into two types. These two types differ in the CRT display synchronizing generator circuits.
Obeserve the printed circuit board. On the lower side board, slightly toward the right form center, there will be a printed sign shown in Fig. 7-1.

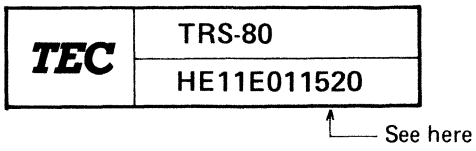


Figure 7-1. PRINTED SIGN ON PRINTED CIRCUIT BOARD

Note the numbers HE11E . . . . below the TRS-80. The difference between the two types related above can be distinguished by noting the second digit from the end. There are those with just the digit number 1 and others with 2 and above. In Fig. 7-1, number 2 is shown. The circuit differences in the two types of TRS-80 is shown in Fig. 7-2 for number 1 and in Fig. 7-3 for number 2 and larger.
In the upper circuit shown in Fig. 7-2, the horizontal synchronizing pulse width, due to dispersion in the parts, differed slightly with each unit. By replacing R60 and other resistors, the differences were confined to within a certain range, but in order to eliminate such process, the circuit was modified to that shown in Fig. 7-3. There is absolutely no difference in performance due to this change.

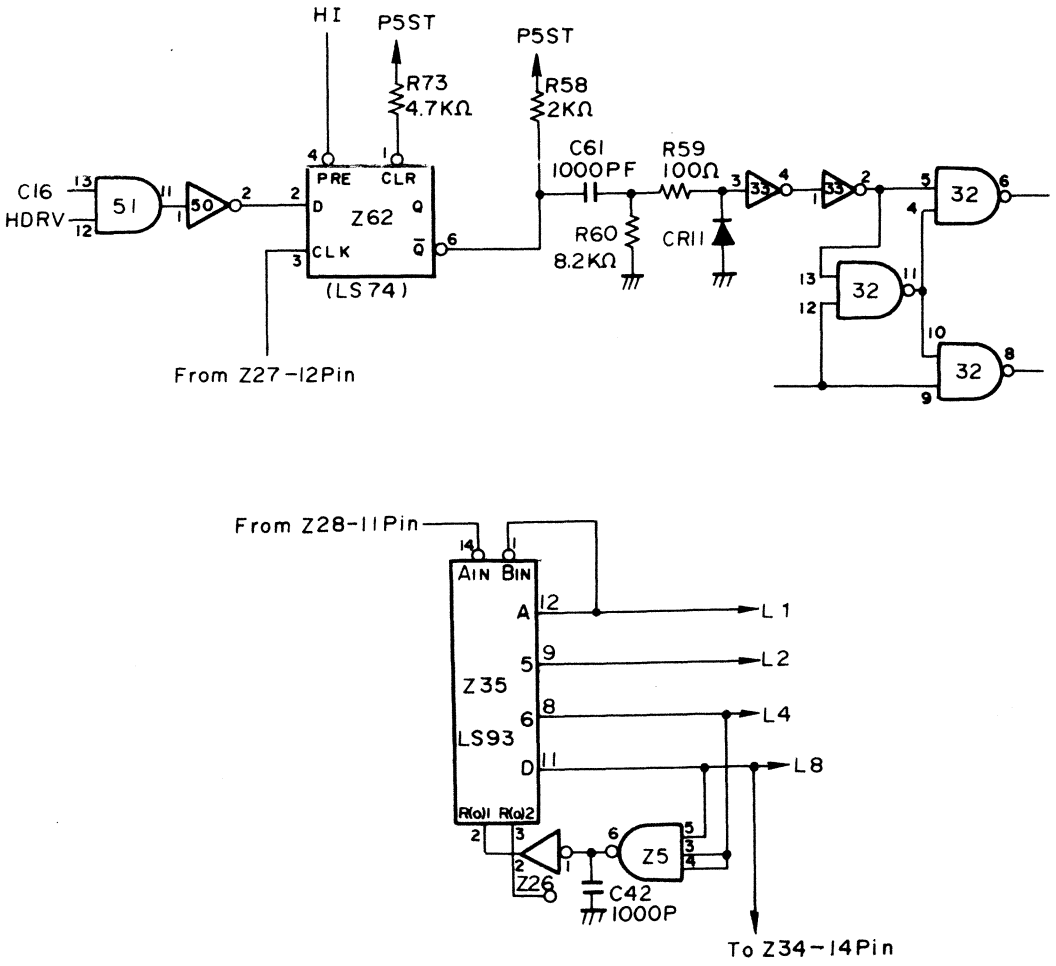


Figure 7-2. CIRCUIT DIFFERENCE BETWEEN TWO TYPES (1)

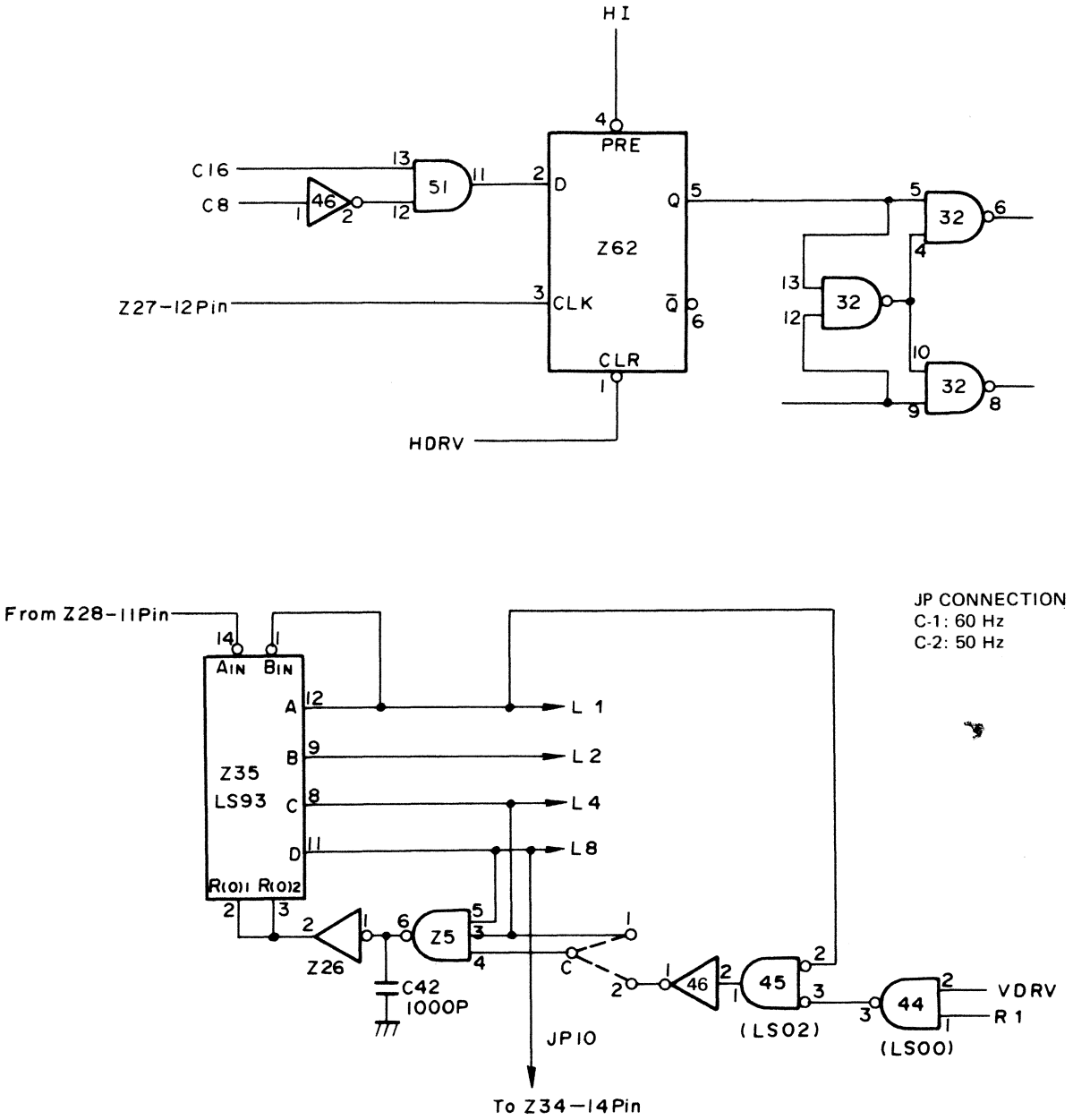


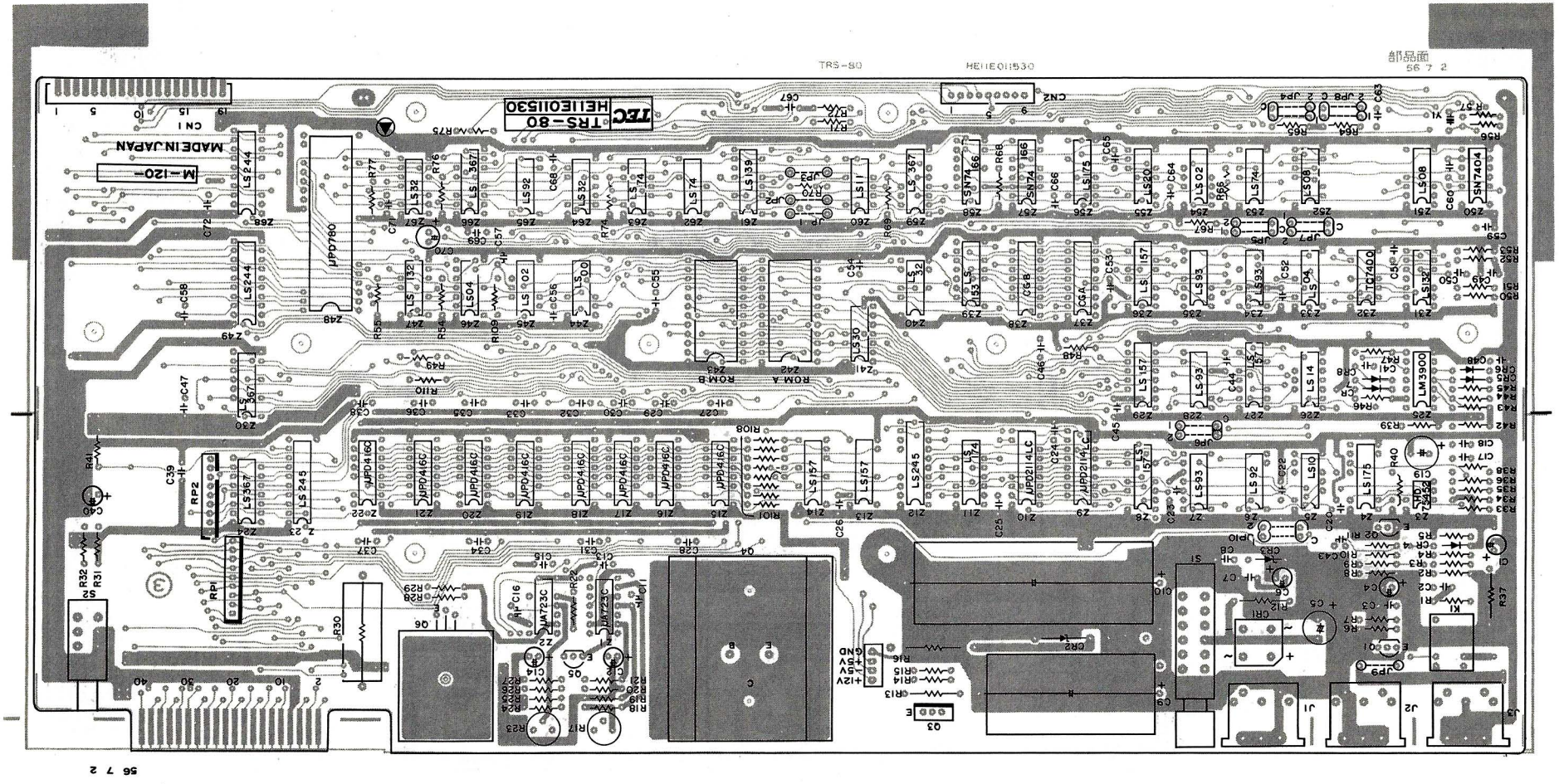
Figure 7-3. CIRCUIT DIFFERENCE BETWEEN TWO TYPES (2)

The difference between Fig. 7-2 and 7-3 in the lower circuits shown, is the method for compensating difference in power frequency. In the products supplied to countries having 50 Hz power supply frequency, the vertical synchronizing frequency has been made to conform with 50 Hz. (In countries with 60 Hz power frequency, the vertical synchronizing frequency has been made to conform with 60 Hz). However, this synchronizing signal generating circuit is initially based on 60 Hz design so that even when jumpers are used to make conversion to 50 Hz, there will still be a frequency difference of about 1 % with 50 Hz. The circuit made to compensate for this is shown in lower part of Fig. 7-3. With the circuit shown in Fig. 7-2, there could be slight shifting the displayed picture in vicinity of power stations.

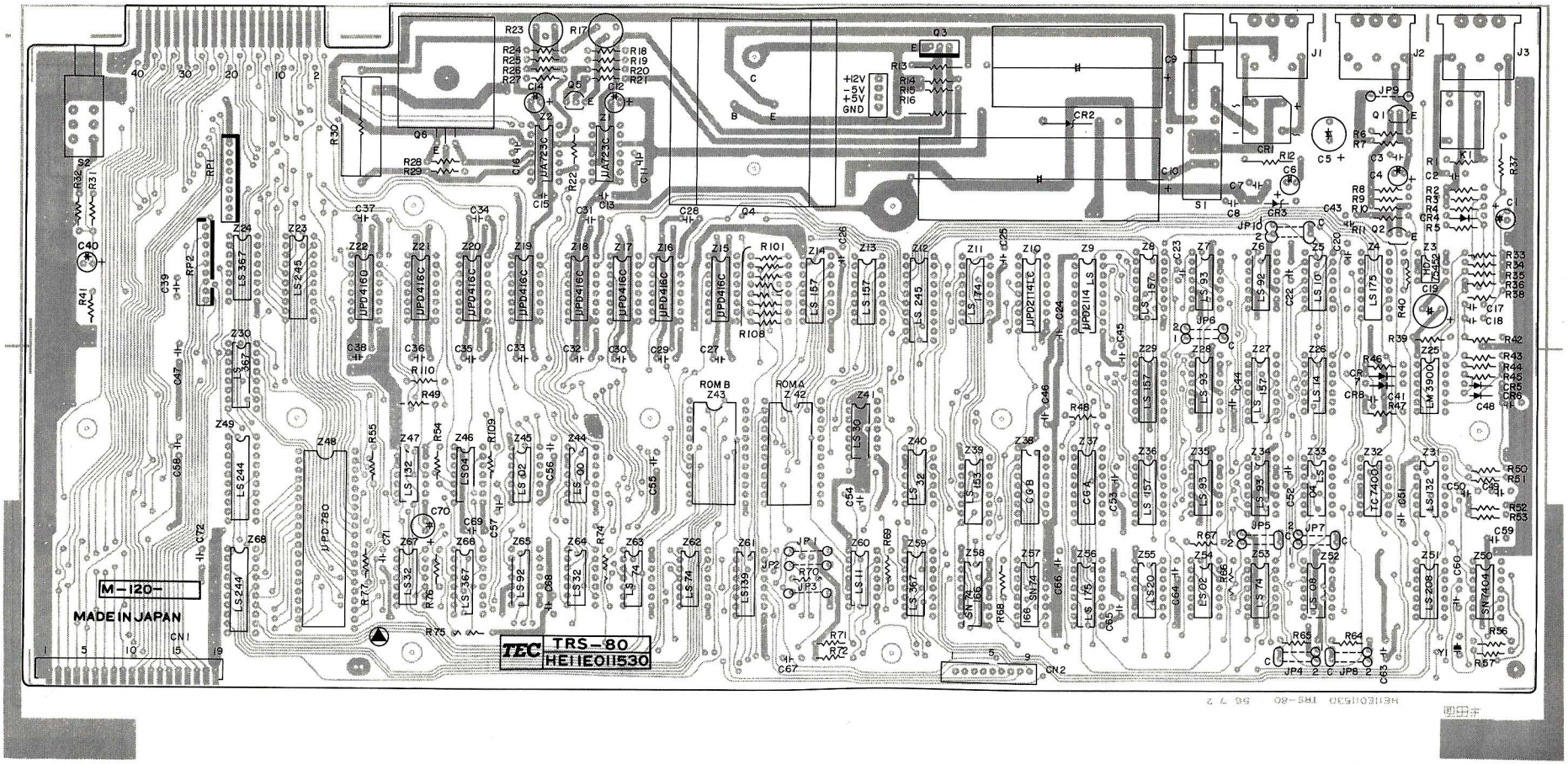
In the circuit shown in Fig. 7-2, replacing the 10.6445 MHz quartz crystal oscillator with 10.4832 MHz type will prevent any picture distortion near power station, but in this case, there will be no 60 Hz conversion when the jumper is changed over to 60 Hz.

In the lower circuit shown in Fig. 7-3, it is no necessary to changing the oscillator as there will be virtually no distortion at 50 Hz and no picture swaying near power transformer. Jumper change-over to 60 Hz can also be made hardly any distortion.
A heavy jumper wire (blue) is soldered to the pin connector part for connecting CPU main body to expansion interface. There is a cut in the GND pattern near the opposite side of the jumper wire. The reason for this is not an error in the GND pattern wiring. The reason for this is that there is a difference in the GND potential at the various parts of the printed circuit board although the difference is small.
Unless supplemented by this pattern cut and jumper wire, when the expansion interface and the CPU are connected together, the mutual incompatibility created by the dispersion in the various components will create RAM errors although the possibilities are small. The components that produce RAM error are not capable of causing the CPU to malfunction or fail to operate. There is difference among these faulty components, some malfunctioning frequently and others very rarely. The above measures are being taken to prevent any trouble from arising beforehand.

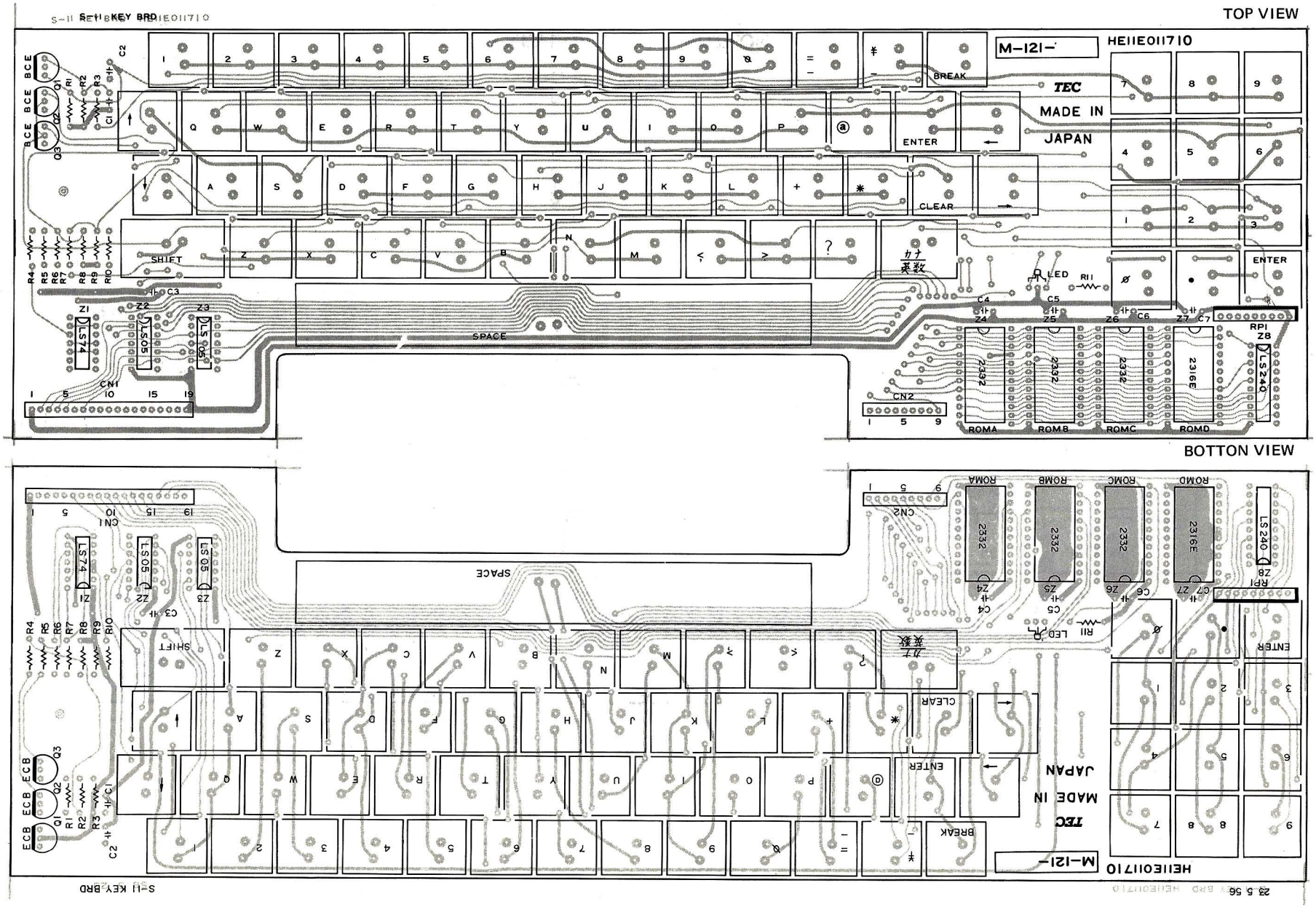
8. PRINTED CIRCUIT BOARD



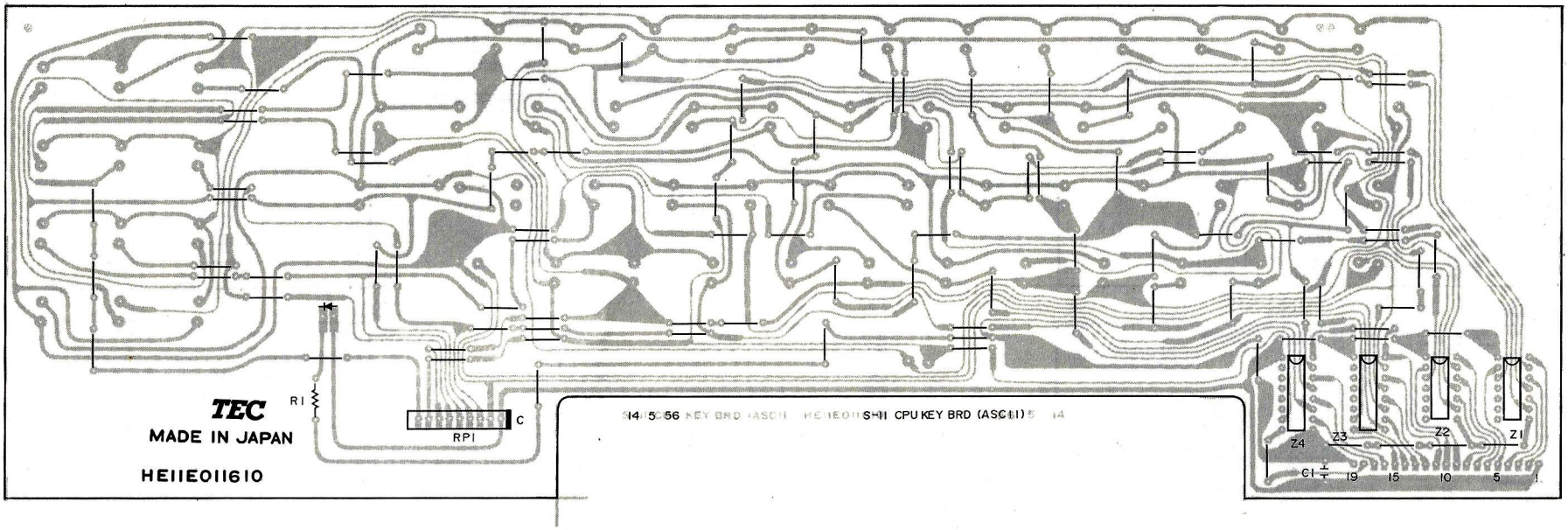
CPU LOGIC PCB (TOP VIEW)



CPU LOGIC PCB (BOTTON VIEW)



KANA KEYBOARD PCB



ASC II KEYBOARD PCB (BOTTON VIEW)

9. PARTS LIST

Ref. No.	Description			Manufacturer Part Number	LEVEL-I	LEVEL-II	LEVEL-II KANA
	TRS-80 MODEL-I CPU PCB Assembly (50 Hz)			HE82D050324	1	0	0
	TRS-80 MODEL-I CPU PCB Assembly (60 Hz)			HE82D050315	1	0	0
	TRS-80 MODEL-I CPU PCB Assembly (50 Hz)			HE82D050322	0	1	0
	TRS-80 MODEL-I CPU PCB Assembly (60 Hz)			HE82D050323	0	1	0
	TRS-80 MODEL-I CPU PCB Assembly (60 Hz)			HE82D050321	0	0	1
	TRS-80 MODEL-I CPU PCB			HE11E011530	1	1	1
	CAPACITORS						
C1	Electrolytic Capacitor	CEUSM1C100	10 μF	24310361020	1	1	1
C2	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C3	Ceramic Capacitor	DB205YB103M	0.01 μF	2426007310M	1	1	1
C4	Electrolytic Capacitor	CEUSM1C100	10 μF	24310361020	1	1	1
C5	Electrolytic Capacitor	CEUSM1C221	220 μF	24310372220	1	1	1
C6	Electrolytic Capacitor	CEUSM1C100	10 μF	24310361020	1	1	1
C7	Ceramic Capacitor	DB205YB103M	0.01 μF	2426007310M	1	1	1
C8	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C9	Electrolytic Capacitor	CEUST1V222	2200 μF	24311582240	1	1	1
C10	Electrolytic Capacitor	TLB1C103MAA	10000 μF	24311991020	1	1	1
C11	Film Capacitor	TDYS1H102K	1000 pF	2426101210K	1	1	1
C12	Electrolytic Capacitor	CEUSM1C100	10 μF	24310361020	1	1	1
C13	Ceramic Capacitor	DB205YB103M	0.01 μF	2426007310M	1	1	1
C14	Electrolytic Capacitor	CEUSM1C100	10 μF	24310361020	1	1	1
C15	Ceramic Capacitor	DB205YB103M	0.01 μF	2426007310M	1	1	1
C16	Film Capacitor	TDYS1H102K	1000 pF	2426101210K	1	1	1
C17	Ceramic Capacitor	DB200YB221K5L5	220 pF	2426000122K	1	1	1
C18	Ceramic Capacitor	DB200YB221K5L5	220 pF	2426000122K	1	1	1
C19	Electrolytic Capacitor	CEUSM1C101	100 μF	24310371020	1	1	1
C20	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C22	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C23	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C24	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C25	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C26	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C27	Ceramic Capacitor	RSB206YD104Z6L5	0.1 μF	24260424100	1	1	1
C28	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C29	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C30	Ceramic Capacitor	RSB206YD104Z6L5	0.1 μF	24260424100	1	1	1
C31	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C32	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C33	Ceramic Capacitor	RSB206YD104Z6L5	0.1 μF	24260424100	1	1	1
C34	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C35	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C36	Ceramci Capacitor	RSB206YD104Z6L5	0.1 μF	24260424100	1	1	1
C37	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C38	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C39	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C40	Electrolytic Capacitor	CEUSM1C100	10 μF	24310361020	1	1	1
C41	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C43	Ceramic Capacitor	DB200YB101K5L5	100 pF	2426000110K	1	1	1
C44	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C45	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C46	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C47	Ceramic Capacitor	RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1

Ref. No.	Description				Manufacturer Part Number	LEVEL-I	LEVEL-II	LEVEL-II KANA
C48	Film Capacitor		TDYS1H102K	1000 pF	2426101210K	1	1	1
C49	Ceramic Capacitor		RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C50	Film Capacitor		CQ92M1H273KA	27000 pF	2426136327K	1	1	1
C51	Ceramic Capacitor		RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C52	Ceramic Capacitor		RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C53	Ceramic Capacitor		RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C54	Ceramic Capacitor		RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C55	Ceramic Capacitor		RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C56	Ceramic Capacitor		RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C57	Film Capacitor		TDYS1H102K	1000 pF	2426101210K	1	1	1
C58	Ceramic Capacitor		RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C59	Ceramic Capacitor		RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C60	Ceramic Capacitor		SDT200SL470J	47 pF	2426012047J	1	1	1
C63	Ceramic Capacitor		RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C64	Ceramic Capacitor		RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C65	Ceramic Capacitor		RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C66	Ceramic Capacitor		RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C67	Ceramic Capacitor		RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C68	Ceramic Capacitor		RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C69	Ceramic Capacitor		RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C70	Electrolytic Capacitor		CEUSM1C220	22 μF	24310362220	1	1	1
C71	Ceramic Capacitor		RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
C72	Ceramic Capacitor		RSB103YD104Z6L5	0.1 μF	24260434100	1	1	1
CN1	Flex Lock	HBLB-19R-1J			24420710002	1	1	1
	Jointer	SMCD-19X37-BDX10			24521000004	1	1	1
CN2	Flex Lock	HBLB-9R-1J			24420710001	0	0	1
	Jointer	SMCD-9X37-BDX10			24521000003	0	0	1
	DIODES & RECTIFIER							
CR1	Bridge Rectifier		S2VB20	200V 2A	2421PS2VB20	1	1	1
CR2	Zener Diode	05Z6.2Y	6.2 V 0.5 W		2421T05Z62Y	1	1	1
CR3	Zener Diode	05Z5.1Y	5.1 V 0.5 W		2421T05Z51Y	1	1	1
CR4	Diode	1S1588	35 V 120 mA		2421T115880	1	1	1
CR5	Diode	1S1588	35 V 120 mA		2421T115880	1	1	1
CR6	Diode	1S1588	35 V 120 mA		2421T115880	1	1	1
CR7	Diode	1S1588	35 V 120 mA		2421T115880	1	1	1
CR8	Diode	1S1588	35 V 120 mA		2421T115880	1	1	1
	JACKS							
J1	Connector	S-I3354#1 (5PD1N)			24420060247	1	1	1
J2	Connector	S-I3354#1 (5PD1N)			24420060247	1	1	1
J3	Connector	S-I3354#1 (5PD1N)			24420060247	1	1	1
JP1	Jumper Wire	R28N (1/4 W) 0.0 Ω			2425000000T	0	1	1
JP2	Jumper Wire	R28N (1/4 W) 0.0 Ω			2425000000T	0	1	1
JP3	Jumper Wire	R28N (1/4 W) 0.0 Ω			2425000000T	0	0	1
JP4	Jumper Wire	R28N (1/4 W) 0.0 Ω			2425000000T	1	1	1
JP5	Jumper Wire	R28N (1/4 W) 0.0 Ω			2425000000T	1	1	1
JP6	Jumper Wire	R28N (1/4 W) 0.0 Ω			2425000000T	1	1	1
JP7	Jumper Wire	R28N (1/4 W) 0.0 Ω			2425000000T	1	1	1
JP8	Jumper Wire	R28N (1/4 W) 0.0 Ω			2425000000T	1	1	1
JP9	Jumper Wire	R28N (1/4 W) 0.0 Ω			2425000000T	1	1	0
JP10	Jumper Wire	R28N (1/4 W) 0.0 Ω			2425000000T	1	1	1
K1	Relay	MZ-5 (HG)			24242000137	1	1	1
	TRANSISTORS							
Q1	Transistor	2SC-1815	5 V 150 mA		2422TC18150	1	1	1
Q2	Transistor	2SA-1015	5 V 150 mA		2422TA10150	1	1	1

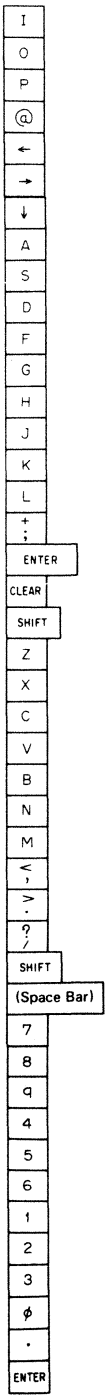
Ref. No.	Description			Manufacturer Part Number	LEVEL-I	LEVEL-II	LEVEL-II KANA
Q3	Transistor	2SC-1449	35 V 3 A	2422NC14490	1	1	1
Q4	Transistor	2SB-531	1000 V 6 A	2422TB53100	1	1	1
	Heat-Sink	6060B		24084246008	1	1	1
	Pan Head Screw	3 x 12	BS (N3C)	24B00140312	2	2	2
	Washer	M3	BS (N3C)	24A62023030	2	2	2
	Spring Washer	M3	PBP (N3C)	24A60043030	2	2	2
	Hexagon Nut	M3	BS (N3C)	24A40070300	1	1	1
Q5	Transistor	2SA-1015	50 V 150 mA	2422TA10150	1	1	1
Q6	Transistor	2SB-595	100 V 5 A	2422TB59500	1	1	1
	Heat-Sink	6106		24084246009	1	1	1
	Pan Head Screw	3 x 12	BS (N3C)	24B00140312	1	1	1
	Washer	M3	BS (N3C)	24A62023030	1	1	1
	Spring Washer	M3	PBP (N3C)	24A60043030	1	1	1
	Hexagon Nut	M3	BS (N3C)	24A40070300	1	1	1
	RESISTORS						
R1	Carbon Resistor		RD1/4PNY 100 Ω ±5%	2425004210T	1	1	1
R2	Carbon Resistor		RD1/4PNY 1.2 kΩ ±5%	2425004312T	1	1	1
R3	Carbon Resistor		RD1/4PNY 7.5 kΩ ±5%	2425004375T	1	1	1
R4	Carbon Resistor		RD1/4PNY 7.5 kΩ ±5%	2425004375T	1	1	1
R5	Carbon Resistor		RD1/4PNY 220 kΩ ±5%	2425004522T	1	1	1
R6	Carbon Resistor		RD1/4PNY 75 Ω ±5%	2425004175T	1	1	1
R7	Carbon Resistor		RD1/4PNY 47 Ω ±5%	2425004147T	1	1	1
R8	Carbon Resistor		RD1/4PNY 330 Ω ±5%	2425004233T	1	1	1
R9	Carbon Resistor		RD1/4PNY 120 Ω ±5%	2425004212T	1	1	1
R10	Carbon Resistor		RD1/4PNY 270 Ω ±5%	2425004227T	1	1	1
R11	Carbon Resistor		RD1/4PNY 10 kΩ ±5%	2425004410T	1	1	1
R12	Carbon Resistor		RD1/2PNY 220 Ω ±5%	24250062222	1	1	1
R13	Carbon Resistor		RD1/2PNY 68 Ω ±5%	24250061682	1	1	1
R14	Carbon Resistor		RD1/4PNY 2.7 kΩ ±5%	2425004327T	1	1	1
R15	Carbon Resistor		RD1/4PNY 750 Ω ±5%	2425004275T	1	1	1
R16	Metal-Oxide Resistor		RS2B 0.33 Ω ±5%	24252219332	1	1	1
R17	Variable Resistor		TM64K 1 kΩ VR	24410460221	1	1	1
R18	Carbon Resistor		RD1/4PNY 1.2 kΩ ±5%	2425004312T	1	1	1
R19	Carbon Resistor		RD1/4PNY 1.2 kΩ ±5%	2425004312T	1	1	1
R20	Carbon Resistor		RD1/4PNY 100 kΩ ±5%	2425004510T	1	1	1
R21	Carbon Resistor		RD1/4PNY 3.3 kΩ ±5%	2425004333T	1	1	1
R22	Carbon Resistor		RD1/4PNY 1.5 kΩ ±5%	2425004315T	1	1	1
R23	Variable Resistor		TM64K 1 kΩ VR	24410460221	1	1	1
R24	Carbon Resistor		RD1/4PNY 3.3 kΩ ±5%	2425004333T	1	1	1
R25	Carbon Resistor		RD1/4PNY 3.3 kΩ ±5%	2425004333T	1	1	1
R26	Carbon Resistor		RD1/4PNY 2.2 kΩ ±5%	2425004322T	1	1	1
R27	Carbon Resistor		RD1/4PNY 12 kΩ ±5%	2425004412T	1	1	1
R28	Carbon Resistor		RD1/4PNY 1.2 kΩ ±5%	2425004312T	1	1	1
R29	Carbon Resistor		RD1/4PNY 2 kΩ ±5%	2425004320T	1	1	1
R30	Metal-Oxide Resistor		RS3B 5.6 Ω ±5%	24252220562	1	1	1
R31	Carbon Resistor		RD1/4PNY 10 kΩ ±5%	2425004410T	1	1	1
R32	Carbon Resistor		RD1/4PNY 100 Ω ±5%	2425004210T	1	1	1
R33	Carbon Resistor		RD1/4PNY 1 MΩ ±5%	2425004610T	1	1	1
R34	Carbon Resistor		RD1/4PNY 10 kΩ ±5%	2425004410T	1	1	1
R35	Carbon Resistor		RD1/4PNY 680 kΩ ±5%	2425004568T	1	1	1
R36	Carbon Resistor		RD1/4PNY 1.8 MΩ ±5%	2425004618T	1	1	1
R37	Carbon Resistor		RD1/2PNY 220 Ω ±5%	24250062222	1	1	1
R38	Carbon Resistor		RD1/4PNY 360 kΩ ±5%	2425004536T	1	1	1
R39	Carbon Resistor		RD1/4PNY 10 Ω ±5%	2425004110T	1	1	1
R40	Carbon Resistor		RD1/4PNY 4.7 kΩ ±5%	2425004347T	1	1	1

Ref. No.	Description			Manufacturer Part Number	LEVEL-I	LEVEL-II	LEVEL-II KANA
R41	Carbon Resistor	RD1/4PNY	4.7 kΩ ±5%	2425004347T	1	1	1
R42	Carbon Resistor	RD1/4PNY	360 kΩ ±5%	2425004536T	1	1	1
R43	Carbon Resistor	RD1/4PNY	560 kΩ ±5%	2425004556T	1	1	1
R44	Carbon Resistor	RD1/4PNY	470 kΩ ±5%	2425004547T	1	1	1
R45	Carbon Resistor	RD1/4PNY	470 kΩ ±5%	2425004547T	1	1	1
R46	Carbon Resistor	RD1/4PNY	470 kΩ ±5%	2425004547T	1	1	1
R47	Carbon Resistor	RD1/4PNY	470 kΩ ±5%	2425004547T	1	1	1
R48	Carbon Resistor	RD1/4PNY	4.7 kΩ ±5%	2425004347T	1	1	1
R49	Carbon Resistor	RD1/4PNY	10 kΩ ±5%	2425004410T	1	1	1
R50	Carbon Resistor	RD1/4PNY	470 kΩ ±5%	2425004547T	1	1	1
R51	Carbon Resistor	RD1/4PNY	1 MΩ ±5%	2425004610T	1	1	1
R52	Carbon Resistor	RD1/4PNY	8.2 kΩ ±5%	2425004382T	1	1	1
R53	Carbon Resistor	RD1/4PNY	8.2 kΩ ±5%	2425004382T	1	1	1
R54	Carbon Resistor	RD1/4PNY	4.7 kΩ ±5%	2425004347T	1	1	1
R55	Carbon Resistor	RD1/4PNY	4.7 kΩ ±5%	2425004347T	1	1	1
R56	Carbon Resistor	RD1/4PNY	910 Ω ±5%	2425004291T	1	1	1
R57	Carbon Resistor	RD1/4PNY	910 Ω ±5%	2425004291T	1	1	1
R64	Carbon Resistor	RD1/4PNY	4.7 kΩ ±5%	2425004347T	1	1	1
R65	Carbon Resistor	RD1/4PNY	4.7 kΩ ±5%	2425004347T	1	1	1
R66	Carbon Resistor	RD1/4PNY	4.7 kΩ ±5%	2425004347T	1	1	1
R67	Carbon Resistor	RD1/4PNY	4.7 kΩ ±5%	2425004347T	1	1	1
R68	Carbon Resistor	RD1/4PNY	4.7 kΩ ±5%	2425004347T	1	1	1
R69	Carbon Resistor	RD1/4PNY	4.7 kΩ ±5%	2425004347T	1	1	1
R70	Carbon Resistor	RD1/4PNY	4.7 kΩ ±5%	2425004347T	1	1	1
R71	Carbon Resistor	RD1/4PNY	4.7 kΩ ±5%	2425004347T	1	1	1
R72	Carbon Resistor	RD1/4PNY	4.7 kΩ ±5%	2425004347T	1	1	1
R74	Carbon Resistor	RD1/4PNY	4.7 kΩ ±5%	2425004347T	1	1	1
R75	Carbon Resistor	RD1/4PNY	330 Ω ±5%	2425004233T	1	1	1
R76	Carbon Resistor	RD1/4PNY	4.7 kΩ ±5%	2425004347T	1	1	1
R77	Carbon Resistor	RD1/4PNY	4.7 kΩ ±5%	2425004347T	1	1	1
R101	Carbon Resistor	RD1/4PNY	330 Ω ±5%	2425004233T	1	1	1
R102	Carbon Resistor	RD1/4PNY	330 Ω ±5%	2425004233T	1	1	1
R103	Carbon Resistor	RD1/4PNY	330 Ω ±5%	2425004233T	1	1	1
R104	Carbon Resistor	RD1/4PNY	330 Ω ±5%	2425004233T	1	1	1
R105	Carbon Resistor	RD1/4PNY	330 Ω ±5%	2425004233T	1	1	1
R106	Carbon Resistor	RD1/4PNY	330 Ω ±5%	2425004233T	1	1	1
R107	Carbon Resistor	RD1/4PNY	330 Ω ±5%	2425004233T	1	1	1
R108	Carbon Resistor	RD1/4PNY	330 Ω ±5%	2425004233T	1	1	1
R109	Carbon Resistor	RD1/4PNY	330 Ω ±5%	2425004233T	1	1	1
R110	Carbon Resistor	RD1/4PNY	330 Ω ±5%	2425004233T	1	1	1
RP1	Resistor Array	EXB-P88472K		24252884721	1	1	1
RP2	Resistor Array	EXB-P88472K		24252884721	1	1	1
S1	Switch	TWA-1570-01-1230		2445B000002	1	1	1
S2	Switch	TWA-1510-01-1230		2445B000001	1	1	1
Y1	Crystal	HC18/U 10.6445 MHz		24240100003	1	1	1
	INTEGRATED CIRCUITS						
Z1	IC	μA723CN		2420SNμA723	1	1	1
Z2	IC	μA723CN		2420SNμA723	1	1	1
Z3	IC	HD75452		2420HD75452	1	1	1
Z4	IC	M74LS175		2420M0LS175	1	1	1
Z5	IC	M74LS10		2420M0LS010	1	1	1
Z6	IC	M74LS92		2420M0LS092	1	1	1
Z7	IC	M74LS93		2420M0LS093	1	1	1
Z8	IC	M74LS157		2420M0LS157	1	1	1
Z9	IC	μPD2114LC		2420NPD2114	1	1	1

Ref. No.	Description	Manufacturer Part Number	LEVEL-I	LEVEL-II	LEVEL-II KANA
Z10	IC μPD2114LC	2420NPD2114	1	1	1
Z11	IC M74LS174	2420M0LS174	1	1	1
Z12	IC M74LS245	2420M0LS245	1	1	1
Z13	IC M74LS157	2420M0LS157	1	1	1
Z14	IC M74LS157	2420M0LS157	1	1	1
Z15	IC μPD416C	2420NPD0416	1	1	1
Z16	IC μPD416C	2420NPD0416	1	1	1
Z17	IC μPD416C	2420NPD0416	1	1	1
Z18	IC μPD416C	2420NPD0416	1	1	1
Z19	IC μPD416C	2420NPD0416	1	1	1
Z20	IC μPD416C	2420NPD0416	1	1	1
Z21	IC μPD416C	2420NPD0416	1	1	1
Z22	IC μPD416C	2420NPD0416	1	1	1
Z23	IC M74LS245	2420M0LS245	1	1	1
Z24	IC M74LS367	2420M0LS367	1	1	1
Z25	IC LM3900	2420LM3900N	1	1	1
Z26	IC M74LS14	2420M0LS014	1	1	1
Z27	IC M74LS157	2420M0LS157	1	1	1
Z28	IC M74LS93	2420M0LS093	1	1	1
Z29	IC M74LS157	2420M0LS157	1	1	1
Z30	IC M74LS367	2420M0LS367	1	1	1
Z31	IC M74LS132	2420M0LS132	1	1	1
Z32	IC TC7400	2420TC07400	1	1	1
Z33	IC M74LS04	2420M0LS004	1	1	1
Z34	IC M74LS93	2420M0LS093	1	1	1
Z35	IC M74LS93	2420M0LS093	1	1	1
Z36	IC M74LS157	2420M0LS157	1	1	1
Z37	Character Generator (Kana) 8046671	2420TNDM009	0	0	1
Z38	Character Generator (ASCII) 8046673	2420TNDM008	1	1	0
Z39	IC M74LS153	2420M0LS153	1	1	1
Z40	IC M74LS32	2420M0LS032	1	1	1
Z41	IC M74LS30	2420M0LS030	1	1	1
Z42	IC 8043032 LEVEL-I M-ROM A	2420TNDM005	1	0	0
	IC 8044364 LEVEL-II M-ROM A	2420TNDM006	0	1	0
	IC Socket C472411 (24P)	24530140000	1	1	0
Z43	IC 8044732 LEVEL-II M-ROM B	2420TNDM007	0	1	0
	IC Socket C472411 (24P)	24530140000	0	1	0
Z44	IC M74LS00	2420M0LS000	1	1	1
Z45	IC M74LS02	2420M0LS002	1	1	1
Z46	IC M74LS04	2420M0LS004	1	1	1
Z47	IC M74LS132	2420M0LS132	1	1	1
Z48	IC μPD780C	2420NPD0780	1	1	1
	IC Socket C474011 (40P)	24530140001	1	1	1
Z49	IC M74LS244	2420M0LS244	1	1	1
Z50	IC SN7404N	2420SN07404	1	1	1
Z51	IC M74LS08	2420M0LS008	1	1	1
Z52	IC M74LS08	2420M0LS008	1	1	1
Z53	IC M74LS74	2420M0LS074	1	1	1
Z54	IC M74LS02	2420M0LS002	1	1	1
Z55	IC M74LS20	2420M0LS020	1	1	1
Z56	IC M74LS175	2420M0LS175	1	1	1
Z57	IC SN74166	2420SN74166	1	1	1
Z58	IC SN74166	2420SN74166	1	1	1
Z59	IC M74LS367	2420M0LS367	1	1	1
Z60	IC M74LS11	2420M0LS011	1	1	1
Z61	IC M74LS139	2420M0LS139	1	1	1

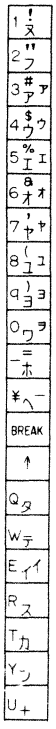
Ref. No.	Description	Manufacturer Part Number	LEVEL-I	LEVEL-II	LEVEL-II KANA
Z62	IC M74LS74	2420M0LS074	1	1	1
Z63	IC M74LS74	2420M0LS074	1	1	1
Z64	IC M74LS32	2420M0LS032	1	1	1
Z65	IC M74LS92	2420M0LS092	1	1	1
Z66	IC M74LS367	2420M0LS367	1	1	1
Z67	IC M74LS32	2420M0LS032	1	1	1
Z68	IC M74LS244	2420M0LS244	1	1	1
	KEY PCB ASCII	HE11E011610	1	1	0
	CAPACITORS				
C1	Ceramic Capacitor RSB103YD104Z6L5 0.01 μF	24260434100	1	1	0
JP1 | JP100	Jumper Wire R28N (1/4 W) 0.0 Ω	2425000000T	1	1	0
	DIODE				
LED	Diode GL-5AR2	2444SGL5AR2	1	1	0
	RESISTOR				
R1	Carbon Resistor RD1/4PNY 330 Ω ±5%	2425004233T	1	1	0
RP1	Resistor Array EXB-P88472K	24252884721	1	1	0
	INTEGRATED CIRCUITS				
Z1	IC M74LS05	2420M0LS005	1	1	0
Z2	IC M74LS05	2420M0LS005	1	1	0
Z3	IC M74LS368	2420M0LS368	1	1	0
Z4	IC M74LS368	2420M0LS368	1	1	0
	Flex Lock HBLB-19R-1J	24420710002	1	1	0
	Assembly ALPS-KEY-SET (ASCII)	2445TNDK002	(65)	(65)	0
	Key Top CM538KM9 ! 1	24460100216	1	1	0
	Key Top CM538KN1 " 2	24460100217	1	1	0
	Key Top CM538KN2 # 3	24460100218	1	1	0
	Key Top CM538KN3 $ 4	24460100219	1	1	0
	Key Top CM538KN4 % 5	24460100220	1	1	0
	Key Top CM538KN5 & 6	24460100221	1	1	0
	Key Top CM538KN6 ' 7	24460100222	1	1	0
	Key Top CM538KN7 (8	24460100223	1	1	0
	Key Top CM538KN8) 9	24460100224	1	1	0
	Key Top CM538KN9 ϕ	24460100225	1	1	0
	Key Top CM538KP1 * :	24460100226	1	1	0
	Key Top CM538KP2 = -	24460100227	1	1	0
	Key Top CN538KP3 BREAK	24460100161	1	1	0
	Key Top CM538GL9 ↑	24460100165	1	1	0
	Key Top CM538GM1 Q	24460100228	1	1	0
	Key Top CM538GM2 W	24460100229	1	1	0
	Key Top CM538GM3 E	24460100230	1	1	0
	Key Top CM538GM4 R	24460100231	1	1	0
	Key Top CM538GM5 T	24460100232	1	1	0
	Key Top CM538GM6 Y	24460100233	1	1	0
	Key Top CM538GM7 U	24460100234	1	1	0

Ref. No.	Description		Manufacturer Part Number	LEVEL-I	LEVEL-II	LEVEL-II KANA
	Key Top	CM538GM8	24460100235	1	1	0
	Key Top	CM538GM9	24460100236	1	1	0
	Key Top	CM538GN1	24460100237	1	1	0
	Key Top	CM538GN2	24460100238	1	1	0
	Key Top	CM538GN3	24460100176	1	1	0
	Key Top	CM538GN4	24460100239	1	1	0
	Key Top	CM537HK7	24460100180	1	1	0
	Key Top	CM538HK8	24460100240	1	1	0
	Key Top	CM538HK9	24460100241	1	1	0
	Key Top	CM538HL1	24460100242	1	1	0
	Key Top	CM538HL2	24460100243	1	1	0
	Key Top	CM538HL3	24460100244	1	1	0
	Key Top	CM538HL4	24460100245	1	1	0
	Key Top	CM538HL5	24460100246	1	1	0
	Key Top	CM538HL6	24460100247	1	1	0
	Key Top	CM538HL7	24460100248	1	1	0
	Key Top	CM538HL8	24460100249	1	1	0
	Key Top	CM532MA2	24460100261	1	1	0
	Key Top	CM538HL9	24460100250	1	1	0
	Key Top	CM537JA5	24460100194	2	2	0
	Key Top	CM538JH9	24460100251	1	1	0
	Key Top	CM538JJ1	24460100252	1	1	0
	Key Top	CM538JJ2	24460100253	1	1	0
	Key Top	CM538JJ3	24460100254	1	1	0
	Key Top	CM538JJ4	24460100255	1	1	0
	Key Top	CM538JJ5	24460100256	1	1	0
	Key Top	CM538JJ6	24460100257	1	1	0
	Key Top	CM538JJ7	24460100258	1	1	0
	Key Top	CM538JJ8	24460100259	1	1	0
	Key Top	CM538JJ9	24460100260	1	1	0
	Key Top	CM5375JA5	24460100194	1	1	0
	Key Top	CM539C87	24460100215	1	1	0
	Key Top	CM538KP4	24460100162	1	1	0
	Key Top	CM538KP5	24460100163	1	1	0
	Key Top	CM538KP6	24460100164	1	1	0
	Key Top	CM538GN5	24460100177	1	1	0
	Key Top	CM533PA1	24460100179	1	1	0
	Key Top	CM538GN7	24460100178	1	1	0
	Key Top	CM538HM1	24460100191	1	1	0
	Key Top	CM538HM2	24460100192	1	1	0
	Key Top	CM538HM3	24460100193	1	1	0
	Key Top	CM538JK1	24460100205	1	1	0
	Key Top	CM538JK2	24460100206	1	1	0
	Key Top	CM538JK3	24460100207	1	1	0
	Panel	CH50340A	24450100223	1	1	0
	Key Switch	KCC10031	24450100222	65	65	0

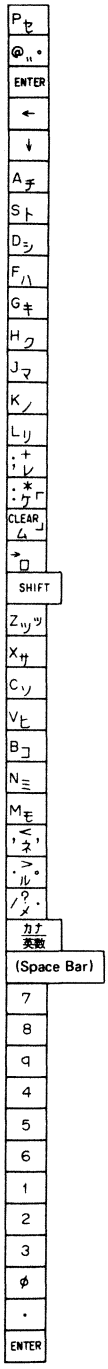


	Key, PC Board (Kana)			HE11E011720	0	0	1
C2	Ceramic Capacitor	RSB103YD104Z6L5	12 V 0.1 μF	24260434100	0	0	1
C3	Ceramic Capacitor	RSB103YD104Z6L5	12 V 0.1 μF	24260434100	0	0	1
C4	Ceramic Capacitor	RSB103YD104Z6L5	12 V 0.1 μF	24260434100	0	0	1
C5	Ceramic Capacitor	RSB103YD104Z6L5	12 V 0.1 μF	24260434100	0	0	1
C6	Ceramic Capacitor	RSB103YD104Z6L5	12 V 0.1 μF	24260434100	0	0	1

Ref. No.	Description			Manufacturer Part Number	LEVEL-I	LEVEL-II	LEVEL-II KANA
C7	Ceramic Capacitor	RSB103YD104Z6L5	12 V 0.1 μF	24260434100	0	0	1
CN1	Flex Lock	HBLB-19R-1J		24420710002	0	0	1
CN2	Flex Lock	HBLB-9R-1J		24420710001	0	0	1
LED	Diode	GL-53RG		24440500001	0	0	1
Q1	Transistor	2SC-1815-GR	5 V 150 mA	2422TC1815G	0	0	1
Q2	Transistor	2SC-1815-GR	5 V 150 mA	2422TC1815G	0	0	1
Q3	Transistor	2SC-1815-GR	5 V 150 mA	2422TC1815G	0	0	1
R1	Carbon Resistor	RD1/4PNY	330 kΩ ±5%	2425004533T	0	0	1
R2	Carbon Resistor	RD1/4PNY	1 kΩ ±5%	2425004310T	0	0	1
R3	Carbon Resistor	RD1/4PNY	100 Ω ±5%	2425004210T	0	0	1
R4	Carbon Resistor	RD1/4PNY	100 kΩ ±5%	2425004510T	0	0	1
R5	Carbon Resistor	RD1/4PNY	100 kΩ ±5%	2425004510T	0	0	1
R6	Carbon Resistor	RD1/4PNY	100 Ω ±5%	2425004210T	0	0	1
R7	Carbon Resistor	RD1/4PNY	330 Ω ±5%	2425004233T	0	0	1
R8	Carbon Resistor	RD1/4PNY	220 Ω ±5%	2425004222T	0	0	1
R9	Carbon Resistor	RD1/4PNY	820 Ω ±5%	2425004282T	0	0	1
R10	Carbon Resistor	RD1/4PNY	4.7 kΩ ±5%	2425004347T	0	0	1
R11	Carbon Resistor	RD1/4PNY	4.7 kΩ ±5%	2425004347T	0	0	1
RP1	Resistor Array	EXB-P88472K		24252884721	0	0	1
RP2	Resistor Array	EXB-P88103K		24252881031	0	0	1
Z1	IC	M74LS74		2420M0LS074	0	0	1
Z2	IC	M74LS05		2420M0LS005	0	0	1
Z3	IC	M74LS05		2420M0LS005	0	0	1
Z4	IC	D2332C-156		2420TNDM001	0	0	1
	IC Socket	C472411 (24P)		24530140000	0	0	1
Z5	IC	8042332		2420TNDM002	0	0	1
	IC Socket	C472411 (24P)		24530140000	0	0	1
Z6	IC	D2332C-160		2420TNDM003	0	0	1
	IC Socket	C472411 (24P)		24530140000	0	0	1
Z7	IC	D2316EC-600		2420TNDM004	0	0	1
	IC Socket	C472411 (24P)		24530140000	0	0	1
Z8	IC	M74LS240		2420M0LS240	0	0	1
	Assembly	ALPS. KEY. SET		2445TNDK001	0	0	(66)
	Key Top	CM538KP7		24460100150	0	0	1
	Key Top	CM538KP8		24460100151	0	0	1
	Key Top	CM538KP9		24460100152	0	0	1
	Key Top	CM538KQ1		24460100153	0	0	1
	Key Top	CM538KQ2		24460100154	0	0	1
	Key Top	CM538KQ3		24460100155	0	0	1
	Key Top	CM538KQ4		24460100156	0	0	1
	Key Top	CM538KQ5		24460100157	0	0	1
	Key Top	CM538KQ6		24460100158	0	0	1
	Key Top	CM538KQ7		24460100159	0	0	1
	Key Top	CM538KQ8		24460100160	0	0	1
	Key Top	CM538KQ9		24460100208	0	0	1
	Key Top	CM538KP3		24460100161	0	0	1
	Key Top	CM538GL9		24460100165	0	0	1
	Key Top	CM538GN8		24460100166	0	0	1
	Key Top	CM538GN9		24460100167	0	0	1
	Key Top	CM538GP1		24460100168	0	0	1
	Key Top	CM538GP2		24460100169	0	0	1
	Key Top	CM538GP3		24460100170	0	0	1
	Key Top	CM538GP4		24460100171	0	0	1
	Key Top	CM538GP5		24460100172	0	0	1
	Key Top	CM538GP6		24460100173	0	0	1
	Key Top	CM538GP7		24460100174	0	0	1



Ref. No.	Description		Manufacturer Part Number	LEVEL-I	LEVEL-II	LEVEL-II KANA
	Key Top	CM538GP8	24460100175	0	0	1
	Key Top	CM538GP9	24460100209	0	0	1
	Key Top	CM538GQ1	24460100210	0	0	1
	Key Top	CM538GN3	24460100176	0	0	1
	Key Top	CM538HK7	24460100180	0	0	1
	Key Top	CM538HM4	24460100181	0	0	1
	Key Top	CM538HM5	24460100182	0	0	1
	Key Top	CM538HM6	24460100183	0	0	1
	Key Top	CM538HM7	24460100184	0	0	1
	Key Top	CM538HM8	24460100185	0	0	1
	Key Top	CM538HM9	24460100186	0	0	1
	Key Top	CM538HN1	24460100187	0	0	1
	Key Top	CM538HN2	24460100188	0	0	1
	Key Top	CM538HN3	24460100189	0	0	1
	Key Top	CM538HN4	24460100190	0	0	1
	Key Top	CM538HN5	24460100211	0	0	1
	Key Top	CM538HN6	24460100212	0	0	1
	Key Top	CM538HN7	24460100213	0	0	1
	Key Top	CM537JA5	24460100194	0	0	1
	Key Top	CM538JK4	24460100195	0	0	1
	Key Top	CM538JK5	24460100196	0	0	1
	Key Top	CM538JK6	24460100197	0	0	1
	Key Top	CM538JK7	24460100198	0	0	1
	Key Top	CM538JK8	24460100199	0	0	1
	Key Top	CM538JK9	24460100200	0	0	1
	Key Top	CM538JL1	24460100201	0	0	1
	Key Top	CM538JL2	24460100202	0	0	1
	Key Top	CM538JL3	24460100203	0	0	1
	Key Top	CM538JL4	24460100204	0	0	1
	Key Top	CM537JA6	24460100214	0	0	1
	Key Top	CM539C87	24460100215	0	0	1
	Key Top	CM538KP4	24460100162	0	0	1
	Key Top	CM538KP5	24460100163	0	0	1
	Key Top	CM538KP6	24460100164	0	0	1
	Key Top	CM538GN5	24460100177	0	0	1
	Key Top	CM533PA1	24460100179	0	0	1
	Key Top	CM538GN7	24460100178	0	0	1
	Key Top	CM538HM1	24460100191	0	0	1
	Key Top	CM538HM2	24460100192	0	0	1
	Key Top	CM538HM3	24460100193	0	0	1
	Key Top	CM538JK1	24460100205	0	0	1
	Key Top	CM538JK2	24460100206	0	0	1
	Key Top	CM538JK3	24460100207	0	0	1
	Key Switch	KCC10031	24450100222	0	0	66
	Panel	CH50340A	24450100223	0	0	1



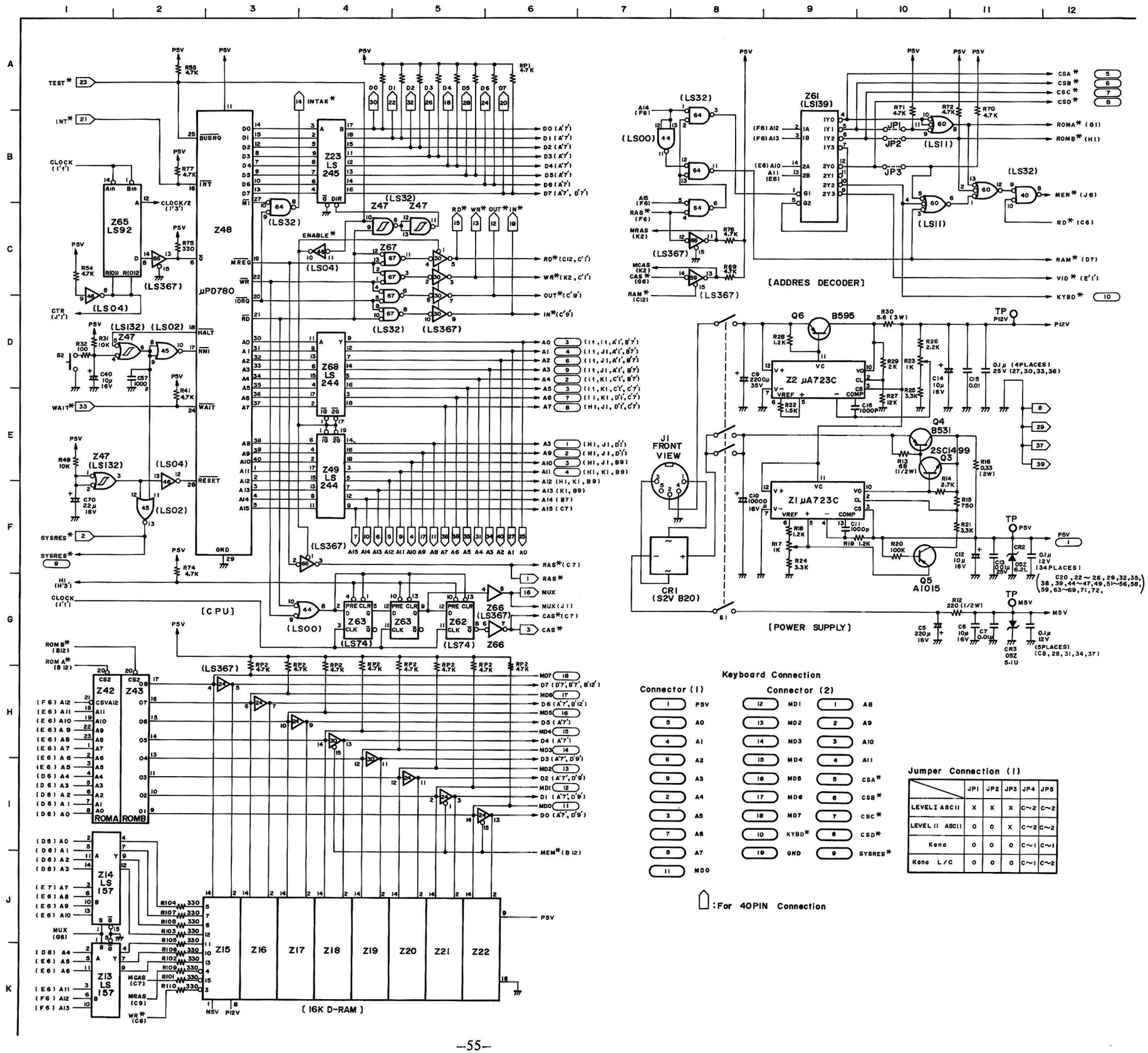
Case (Top)	2408TND0002	1	1	1
Case (Bottom)	2408TND0003	1	1	1
Connector Plate (Door)	2408TND0004	1	1	1
Bezzel	2408TND0005	1	1	1
DIN Connector Cover	2442T000001	1	1	1
Spacer 9ϕ x 11.5 m/m	HE08B016610	1	1	1
Spacer 9ϕ x 9 m/m	HE0BB016510	6	6	6

Ref. No.	Description	Manufacturer Part Number	LEVEL-I	LEVEL-II	LEVEL-II KANA
	Spacer 9ϕ x 18 m/m	HE08B017200	2	2	2
	Rubber Feet SJ-5003	24020710002	4	4	4
	Label 26-1003A	HE09B049513	1	0	0
	Label 26-1006A	HE09B049512	0	1	0
	Label 26-7016A	HE09B049511	0	0	1
	Self Tap Screw 3.5 x 38-FE-STS-B0	24A10563538	2	2	2
	Self Tap Screw 3.5 x 45-FE-STS-B0	24A10563545	2	2	2
	Self Tap Screw 3.5 x 50-FE-STS-B0	24A10563550	2	2	2
	Label Open Case (ASCII)	HE09B049800	1	1	0
	Label Open Case (Kana)	HE09B049700	0	0	1
	Label Warranty	HE09B049600	1	1	1
	Power Supply 100 V	2408TND0014	0	0	1
	Cassette Cable DIN	2408TND0010	1	1	1
	Power Supply 120 V	2408TND0021	1	1	0
	Power Supply 220 V	2408TND0022	1	1	0

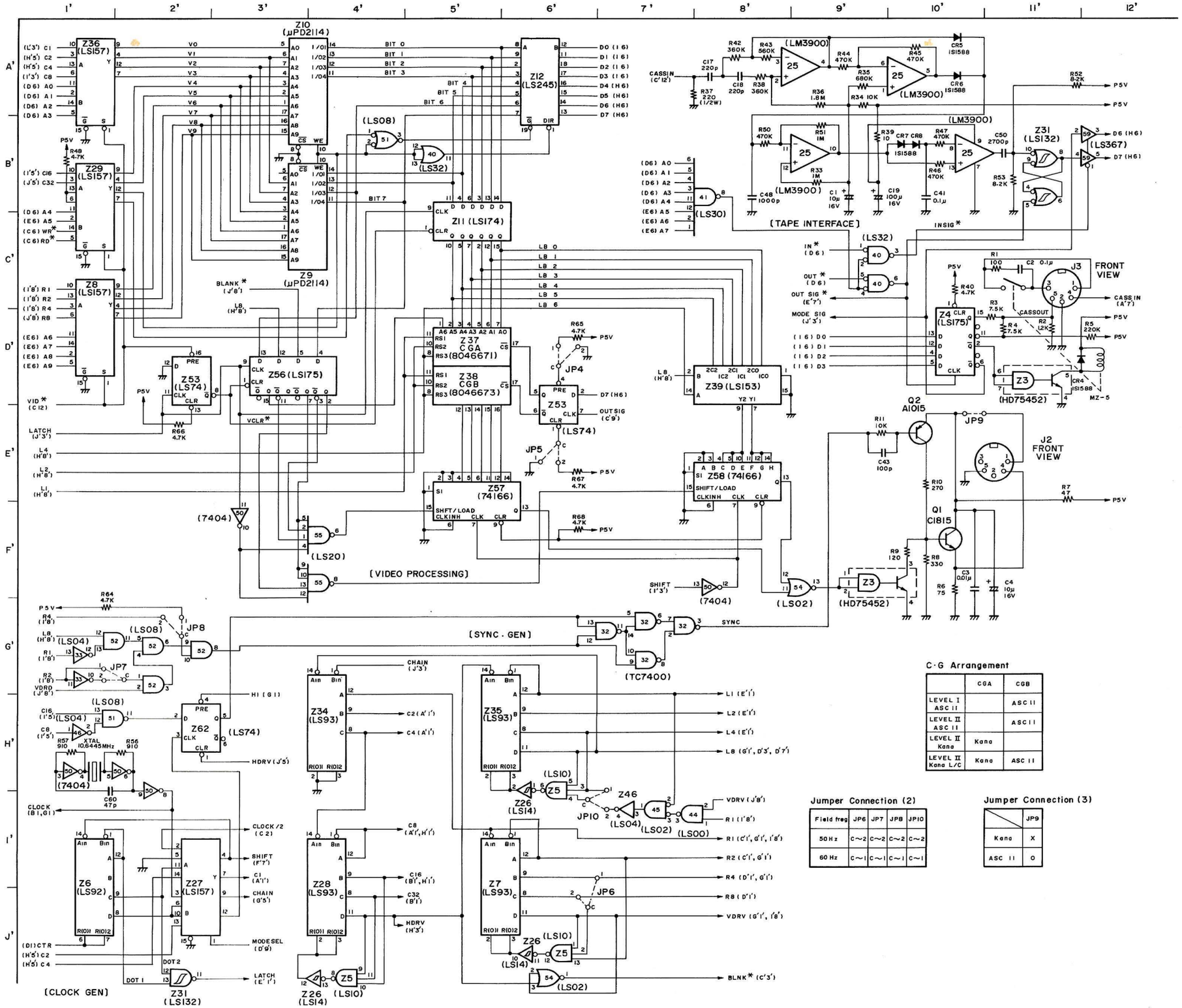
TRS-80 MODEL I PARTS LIST (FOR PCB NO. HE11E011510 only)

Ref. No.	Description			Manufacturer Part Number	LEVEL-I	LEVEL-II	LEVEL-II KANA
	CPU PWB			HE11E011510	1	1	1
	CAPACITORS						
C21	Ceramic Capacitor	DB201YB102K5L5	1000 pF	2426002210K	1	1	1
C42	Ceramic Capacitor	DB201YB102K5L5	1000 pF	2426002210K	1	1	1
C61	Film Capacitor	TDYS1H102K	1000 pF	2426101210K	1	1	1
C62	Film Capacitor	CQ92M1H273KA	27000 pF	2426136327K	1	1	1
CN-1	Jointer	JPS-19-018-33-5		24521000001	1	1	1
CN-2	Jointer	JPS-9-018-33-5		24521000002	0	0	1
	Wafer Assembly	3022-08A		24421080324	1	1	4
CN1	Connector	FJ-19-002		24420780056	1	1	1
CN2	Connector	FJ-9-002		24420780055	0	0	1
	Kana Keyboard	Sub PCB		HE11B005900	0	0	1
	Wafer Assembly	3022-10A		24421080325	0	0	2
	DIODES						
CR9	Diode	1S1588		2421T115880	1	1	1
CR10	Diode	1S1588		2421T115880	1	1	1
CR11	Diode	1S1588		2421T115880	1	1	1
	RESISTORS						
R58	Carbon Resistor	RD1/4PNY	2 kΩ ±5%	2425004320T	1	1	1
R59	Carbon Resistor	RD1/4PNY	100 kΩ ±5%	2425004210T	1	1	1
R60	Carbon Resistor	RD1/4PNY	8.2 kΩ ±5%	2425004382T	1	1	1
R61	Carbon Resistor	RD1/4PNY	100 kΩ ±5%	2425004210T	1	1	1
R62	Carbon Resistor	RD1/4PNY	10 kΩ ±5%	2425004410T	1	1	1
R63	Carbon Resistor	RD1/4PNY	2 kΩ ±5%	2425004320T	1	1	1
R73	Carbon Resistor	RD1/4PNY	4.7 kΩ ±5%	2425004347T	1	1	1

10. SCHEMATIC DIAGRAM (CPU CIRCUIT)



	JP1	JP2	JP3	JP4	JP5
LEVEL I ASCII	X	X	X	C~2	C~2
LEVEL II ASCII	O	O	X	C~2	C~2
Kana	O	O	O	C~1	C~1
Kana L/C	O	O	O	C~1	C~2

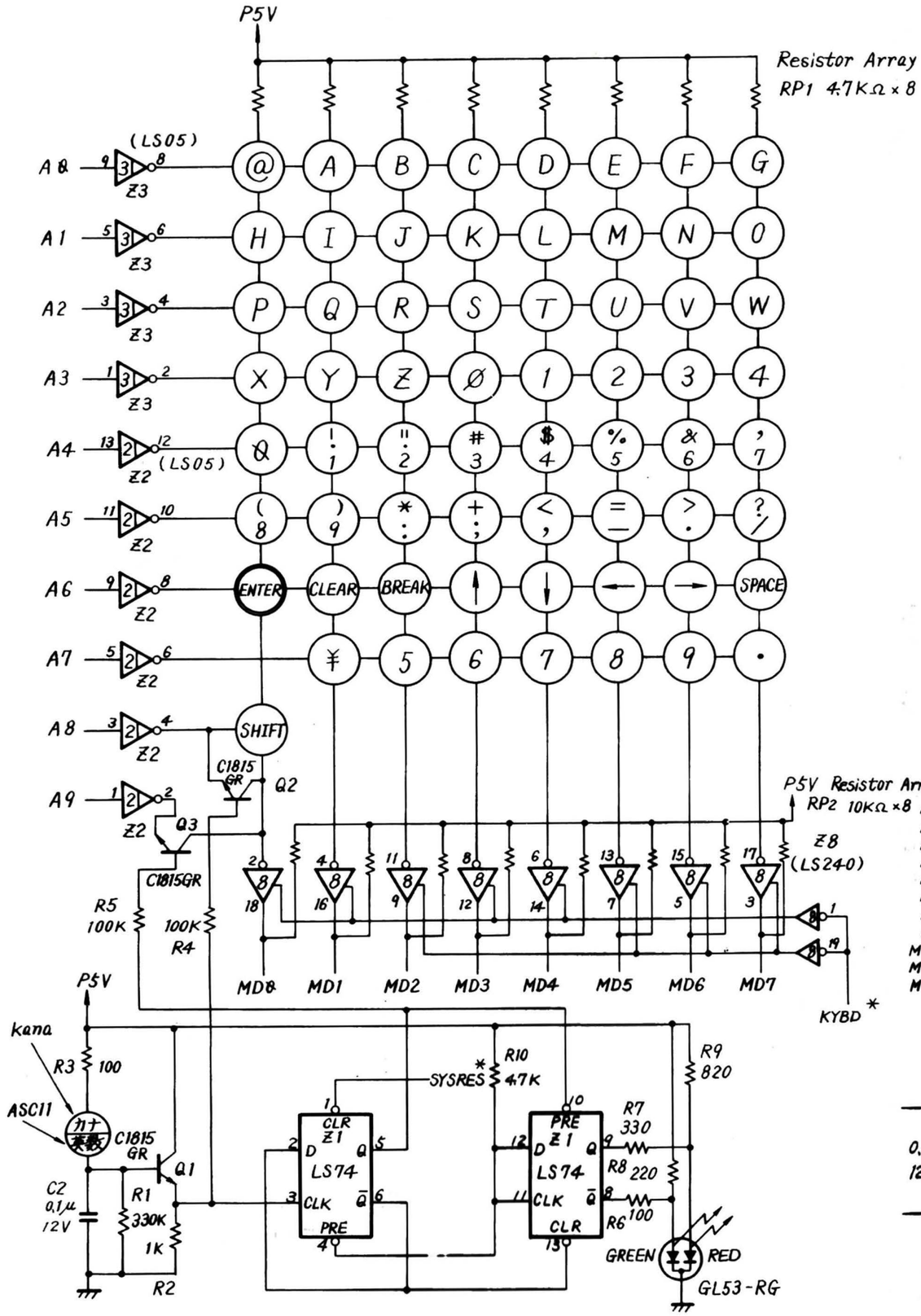


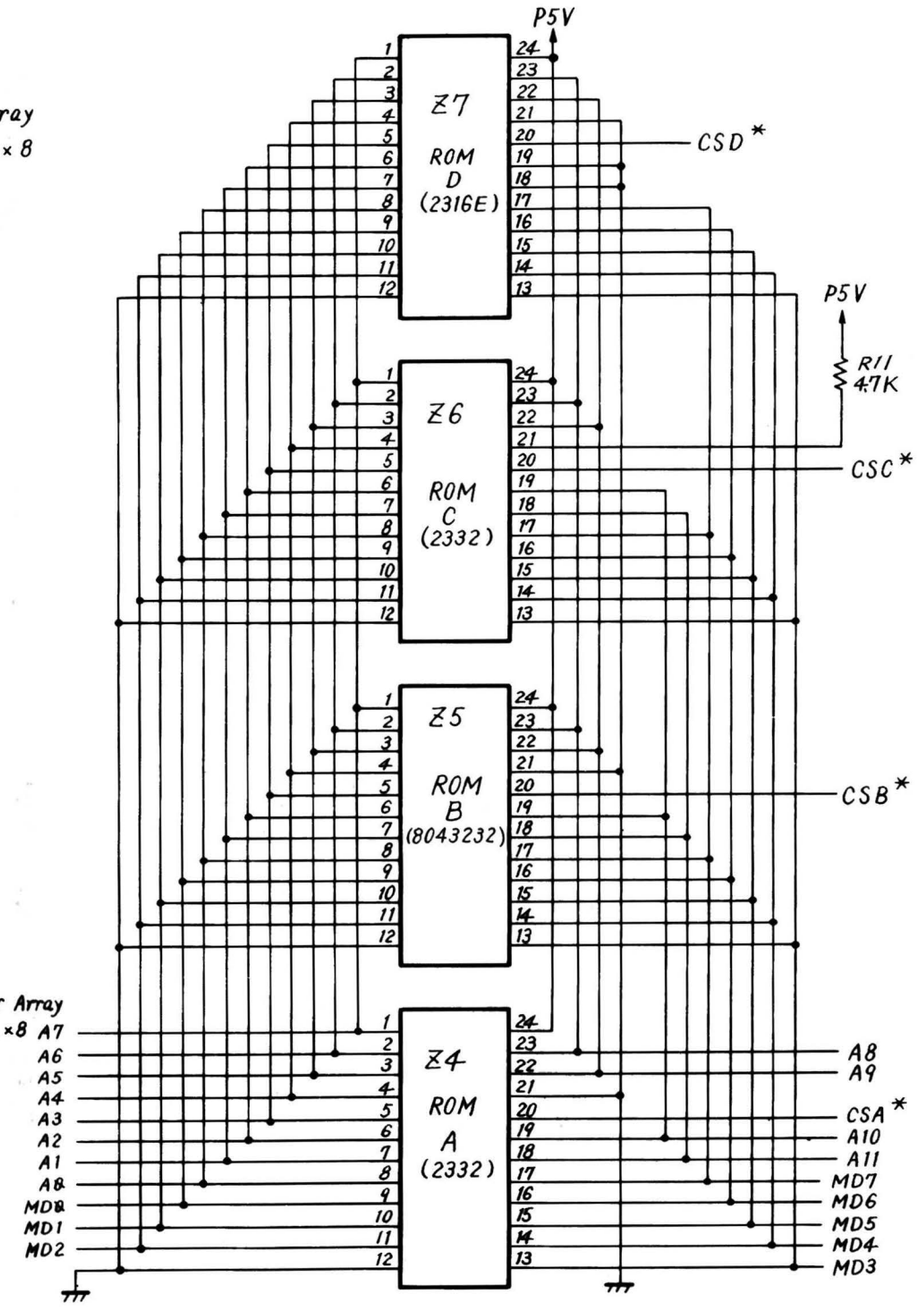
	CGA	CGB
LEVEL I ASC II		ASC II
LEVEL II ASC II		ASC II
LEVEL II Kana	Kana	
LEVEL II Kana L/C	Kana	ASC II

Field freq	JP6	JP7	JP8	JP10
50 Hz	C~2	C~2	C~2	C~2
60 Hz	C~1	C~1	C~1	C~1

	JP9
Kana	X
ASC II	O

11. SCHEMATIC DIAGRAM



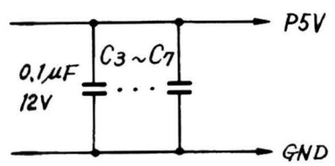


Connector (1)

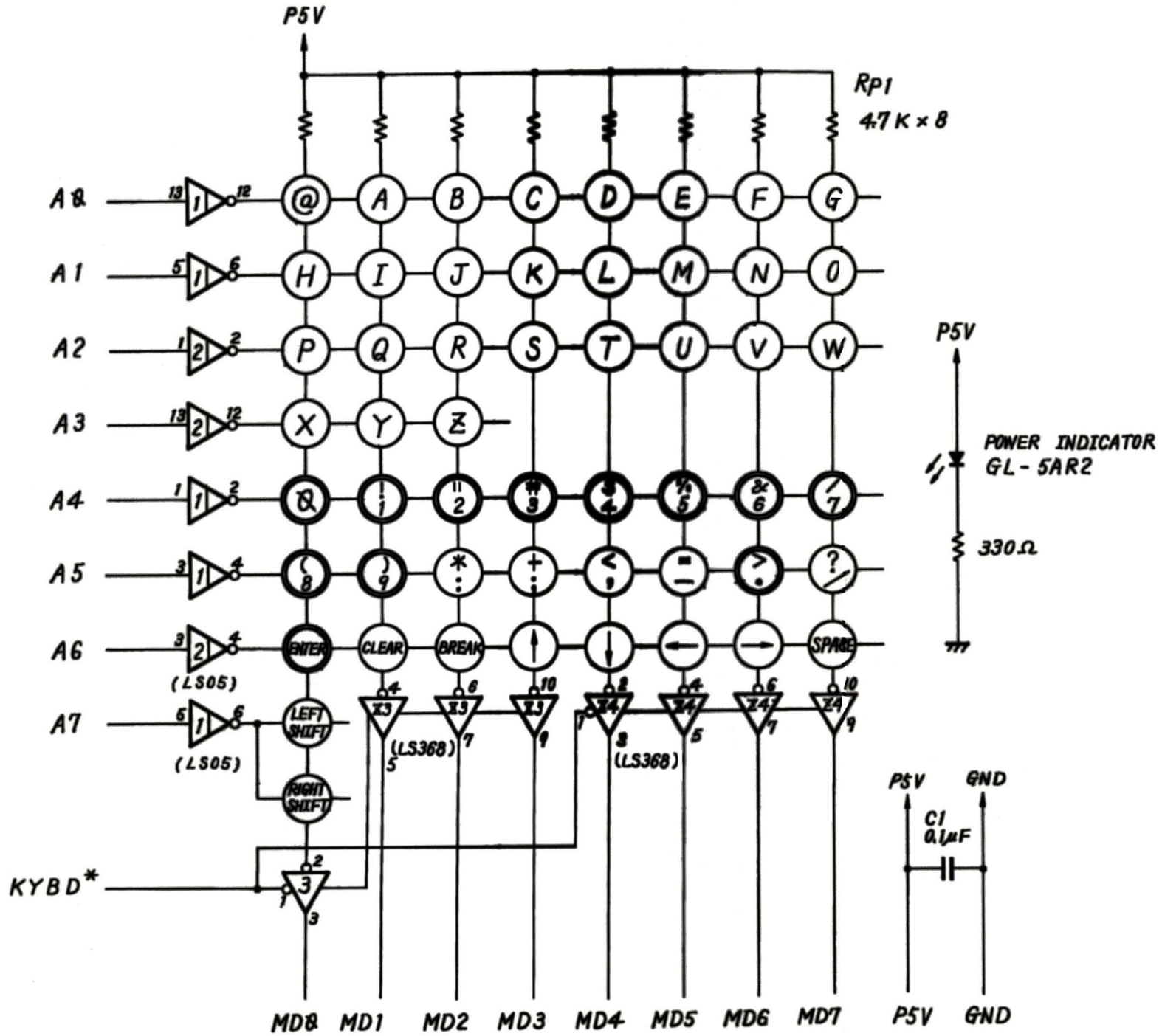
1	P5V
5	A8
4	A1
6	A2
9	A3
2	A4
3	A5
7	A6
8	A7
11	MD8
12	MD1
13	MD2
14	MD3
15	MD4
16	MD5
17	MD6
18	MD7
10	KYBD *
19	GND

Connector (2)

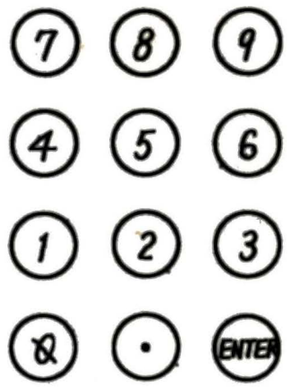
1	A8
2	A9
3	A10
4	A11
5	CSA *
6	CSB *
7	CSC *
8	CSD *
9	SYSRES *



Note : ENTER KEY is Connected Parallel with Main KEY.



TEN KEY



Connector 1

1	P5ST	12	MD1
5	A8	13	MD2
4	A1	14	MD3
6	A2	15	MD4
9	A3	16	MD5
2	A4	17	MD6
3	A5	18	MD7
7	A6	10	KYBD*
8	A7	19	GND
11	MD8		

Note : TEN KEY is Connected Parallel with Main KEY.